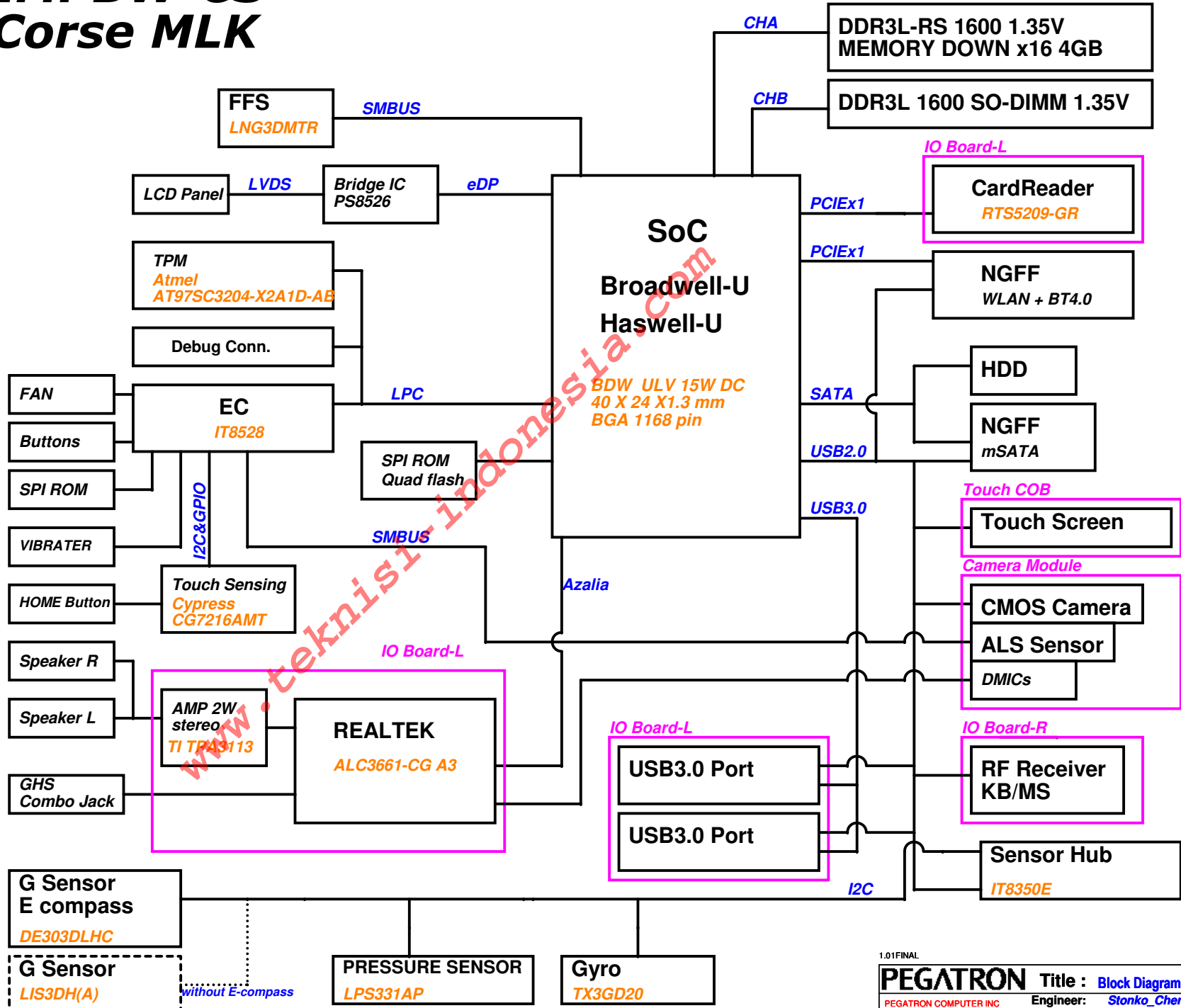


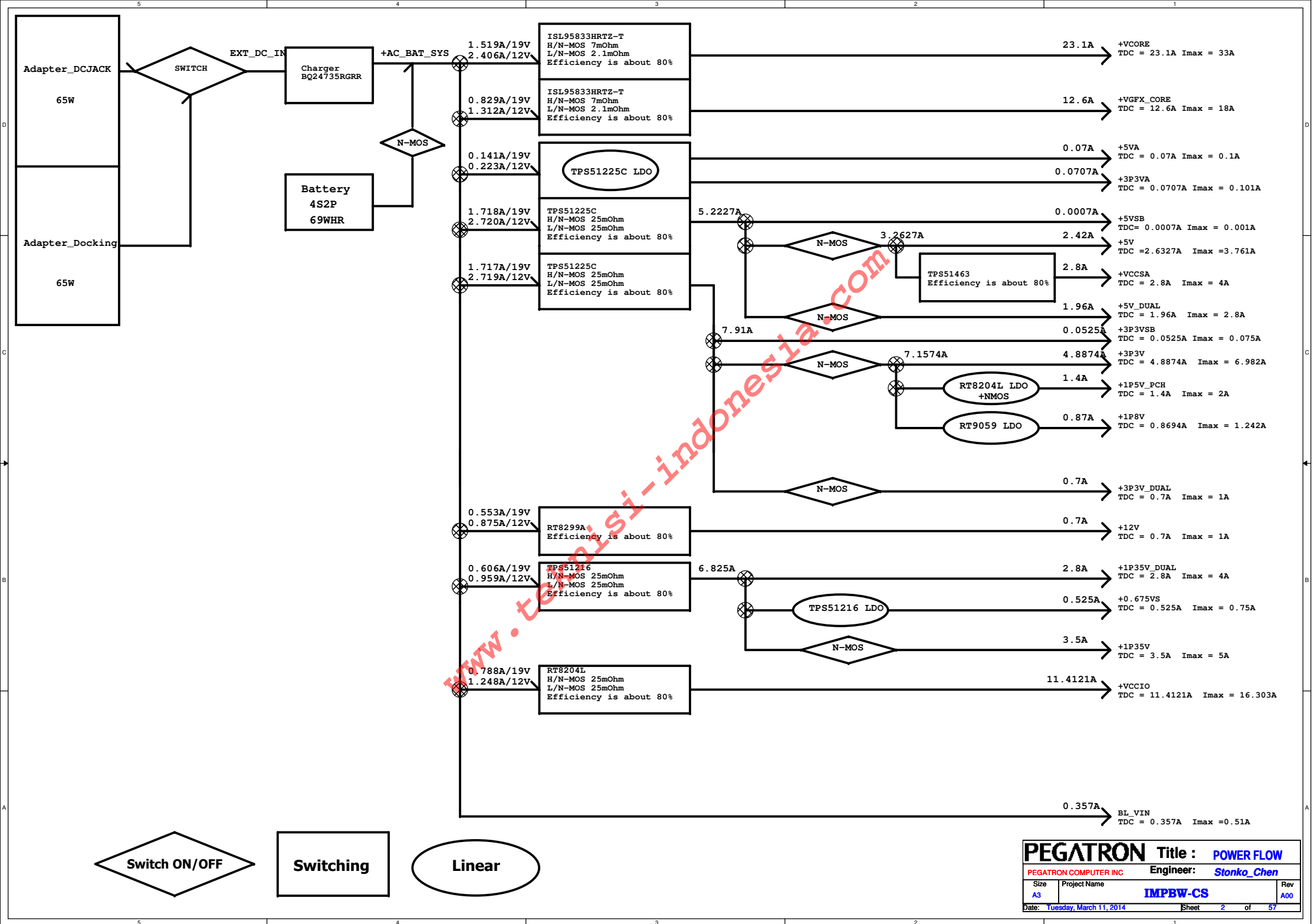
SYSTEM PAGE REF.

01. Block Diagram
02. POWER FLOW
03. Power On Sequence
04. Power On Timing
05. CPU(1)_MISC.JTAG,DDI.EDP
06. CPU(2)_DDR3L-RS
07. CPU(3)_HSW POWER
08. CPU(4)_GND
09. CPU(5)_RESERVED
10. CPU(6)_XDP
11. DDR3L-RS_Memory Down
12. DDR3L-RS_SO-DIMM
13. DDR3L-RS_Decoupling
14. DDR3L-RS_CA/DQ Voltage
15. PCH_SATA, IHDA, RTC
16. PCH_CLK, SMB, LPC
17. PCH_FDI, DMI, SYS PWR
18. PCH_DP, PCI
19. PCH_PCIE, NVRAM, USB
20. PCH_CPU, GPIO, MISC
21. PCH_POWER, GND
22. PCH_SPI, SMB
23. shippingmode
24. NGFF_CARD_WLAN
25. NGFF_CARD_mSATA
26. SATA redriver
27. SATA conn
28. eDP_ANX1122
29. LVDS
30. USB3.0 redriver
31. USB Touch
32. ALS, CAMERA, DMIC
33. RIO LIO connector
34. Homekey_connector
35. Sensor_Hub_IT8350E
36. Gyro&G&Pressure-sensor
37. FFS
38. ITE 8528-1
39. ITE 8528-2
40. TPM
41. VIBRATER
42. THERMAL / FAN
43. RST_Reset Circuit
44. BUG_Debug
45. DSG_Discharge
46. SCREW HOLE
47. POWER_PROTECT
48. DC_DC/BAT CONN
49. DC IN
50. +AC_BAT_SYS & Charger
51. +VCORE
52. +VCORE1
53. +3P3VSB/+5VSB
54. +1P35V_DUAL/+VTT_DDR
55. +1P05V
56. +1P5V
57. Switch

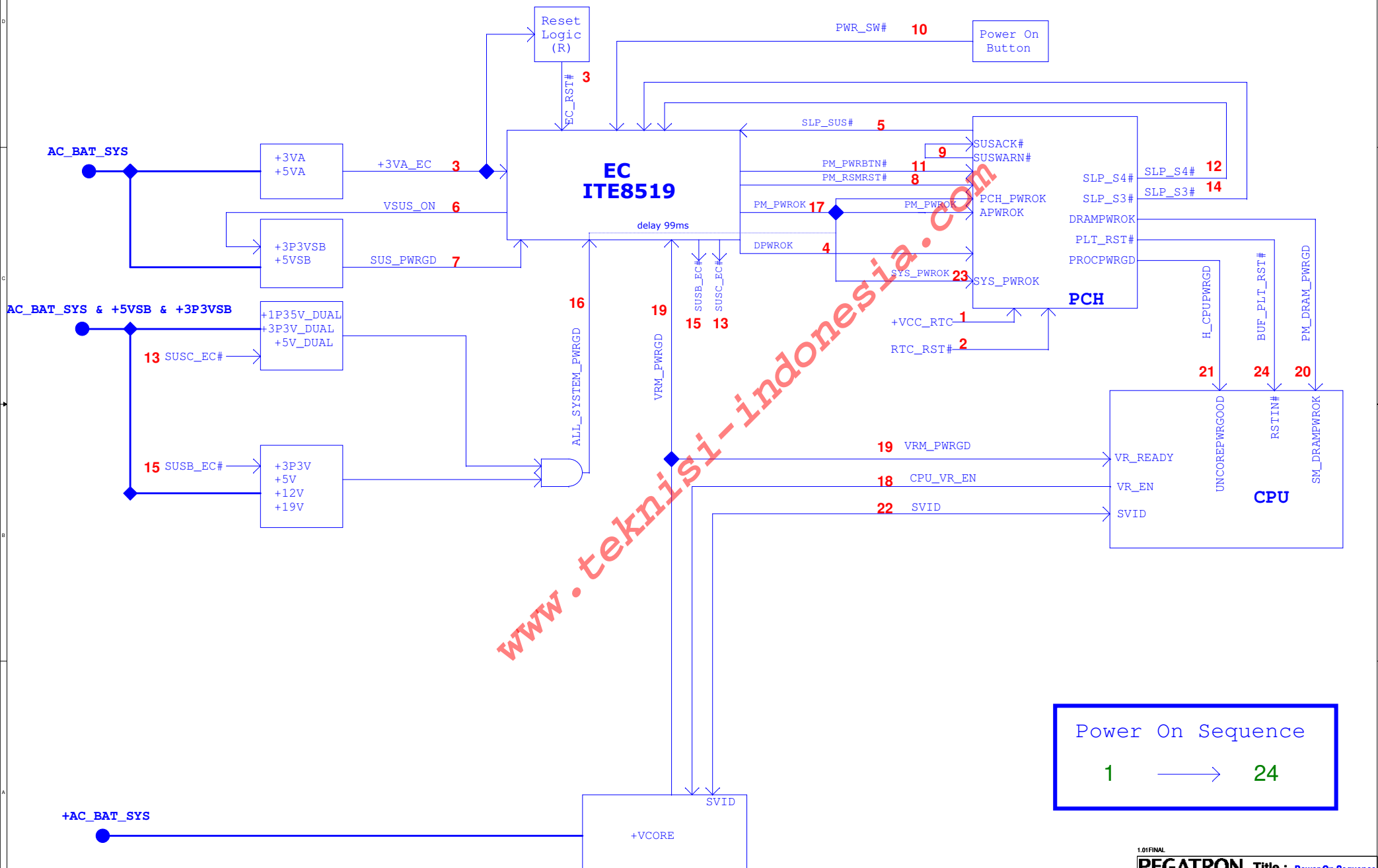
IMPBW-CS Corse MLK

Block Diagram





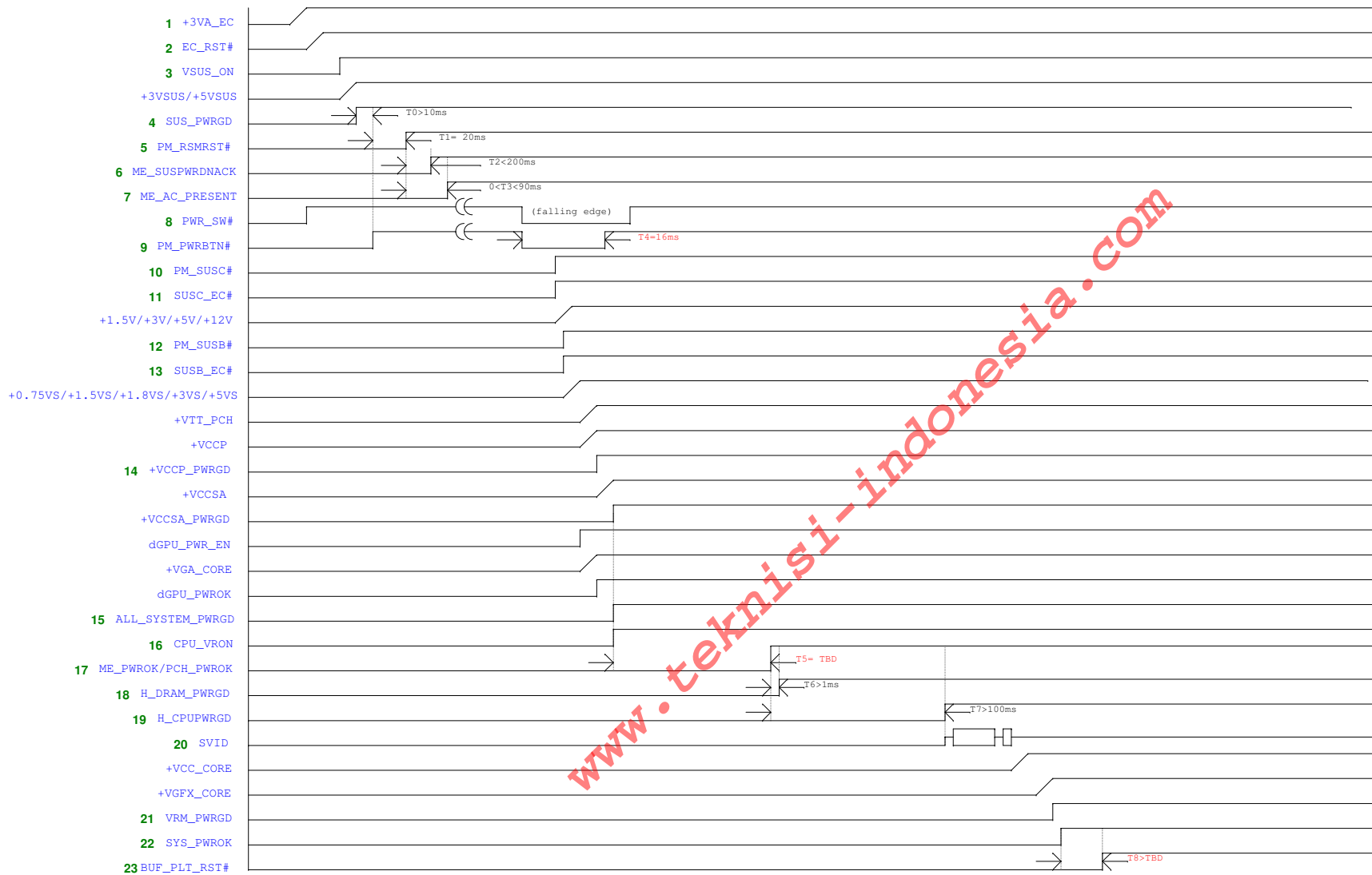
Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)



Power On Sequence

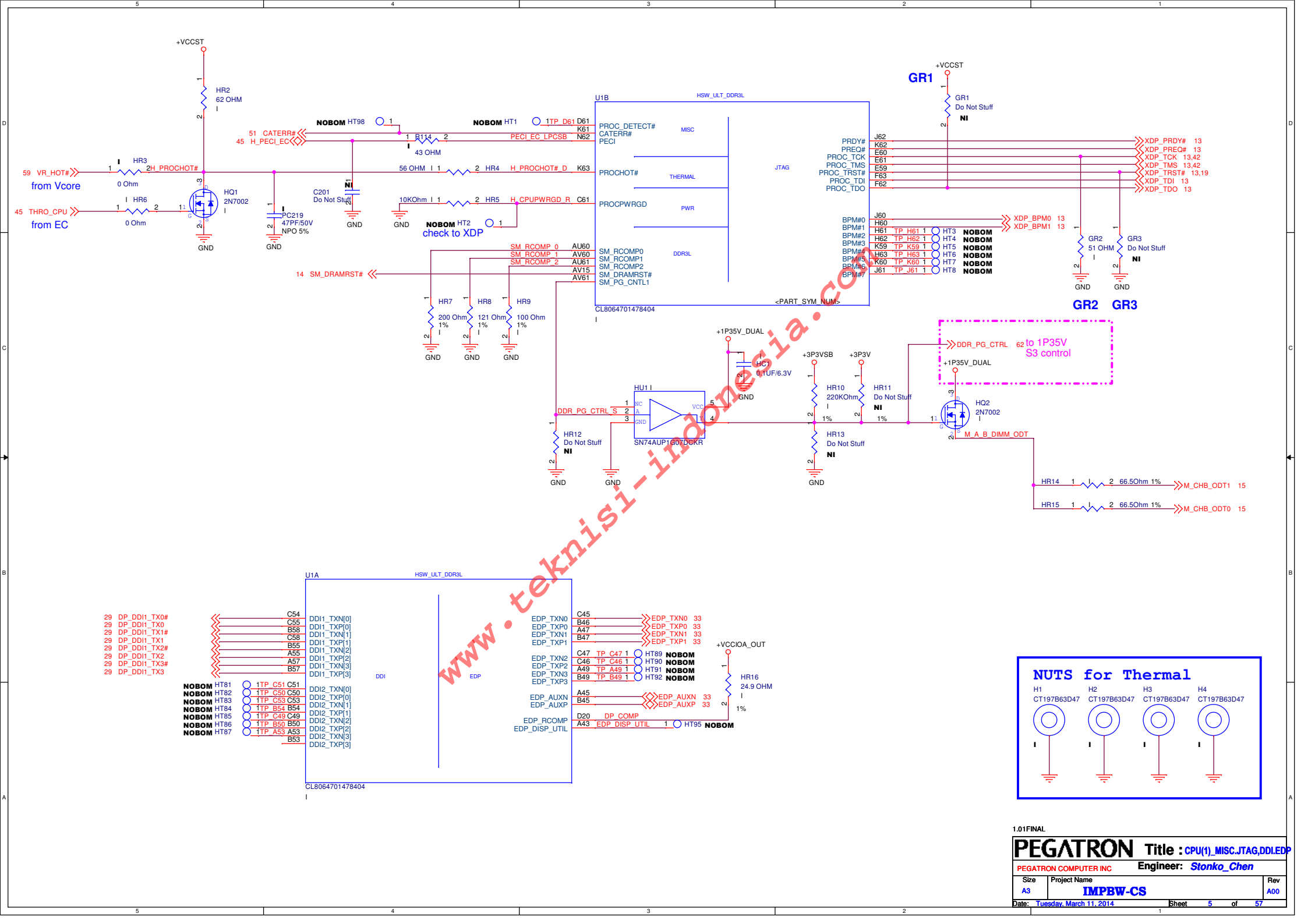
1 → 24

Power On Sequence Diagram G3-S0 R0.3 (non-iAMT, non-Deep Sx)



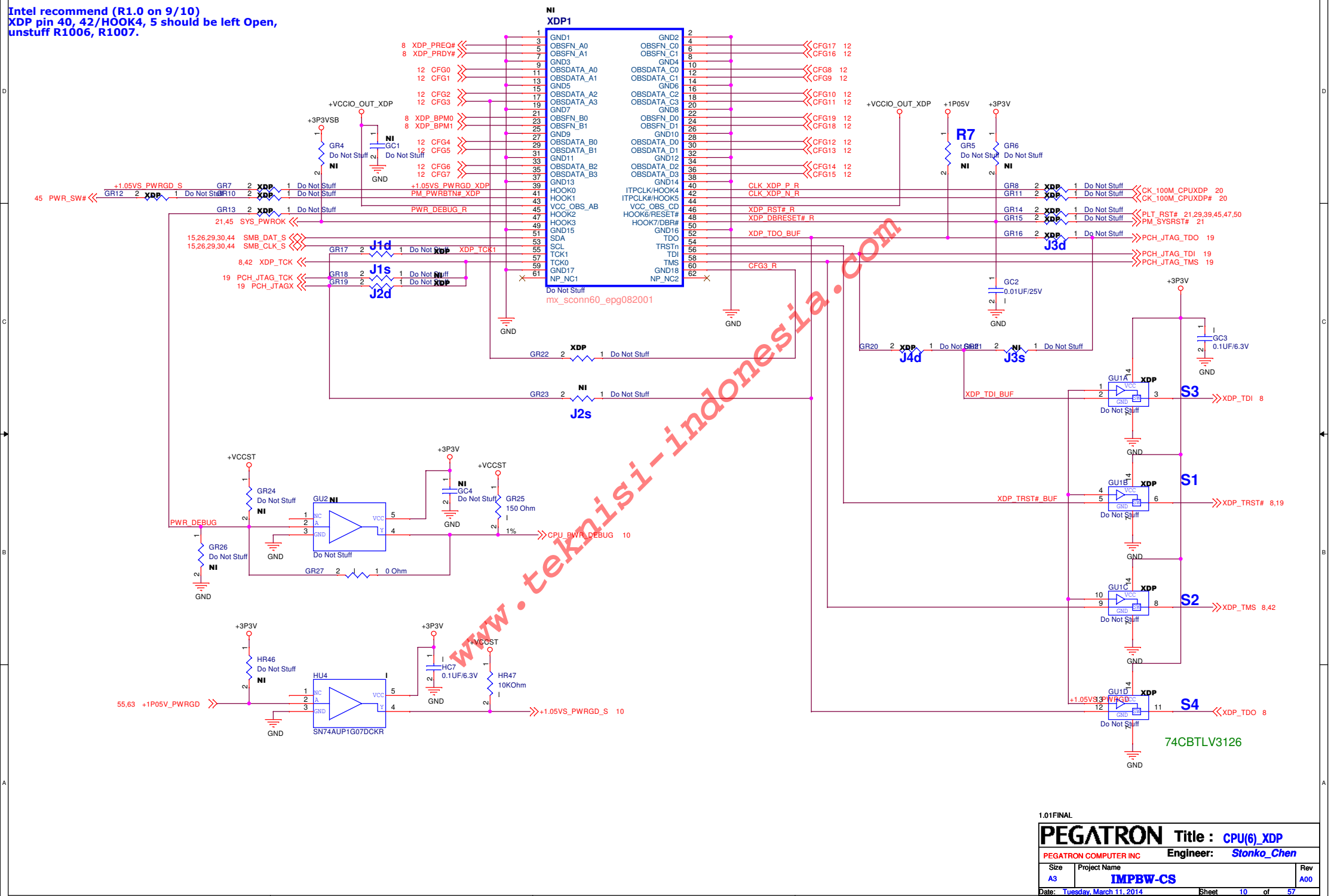
1.01 FINAL

PEGATRON		Title : Power On Timing	
PEGATRON COMPUTER INC		Engineer: Stonko.Chen	
Size	Project Name		Rev
C	IMPBW-CS		A00
Date: Tuesday, March 11, 2014		Sheet	4 of 57

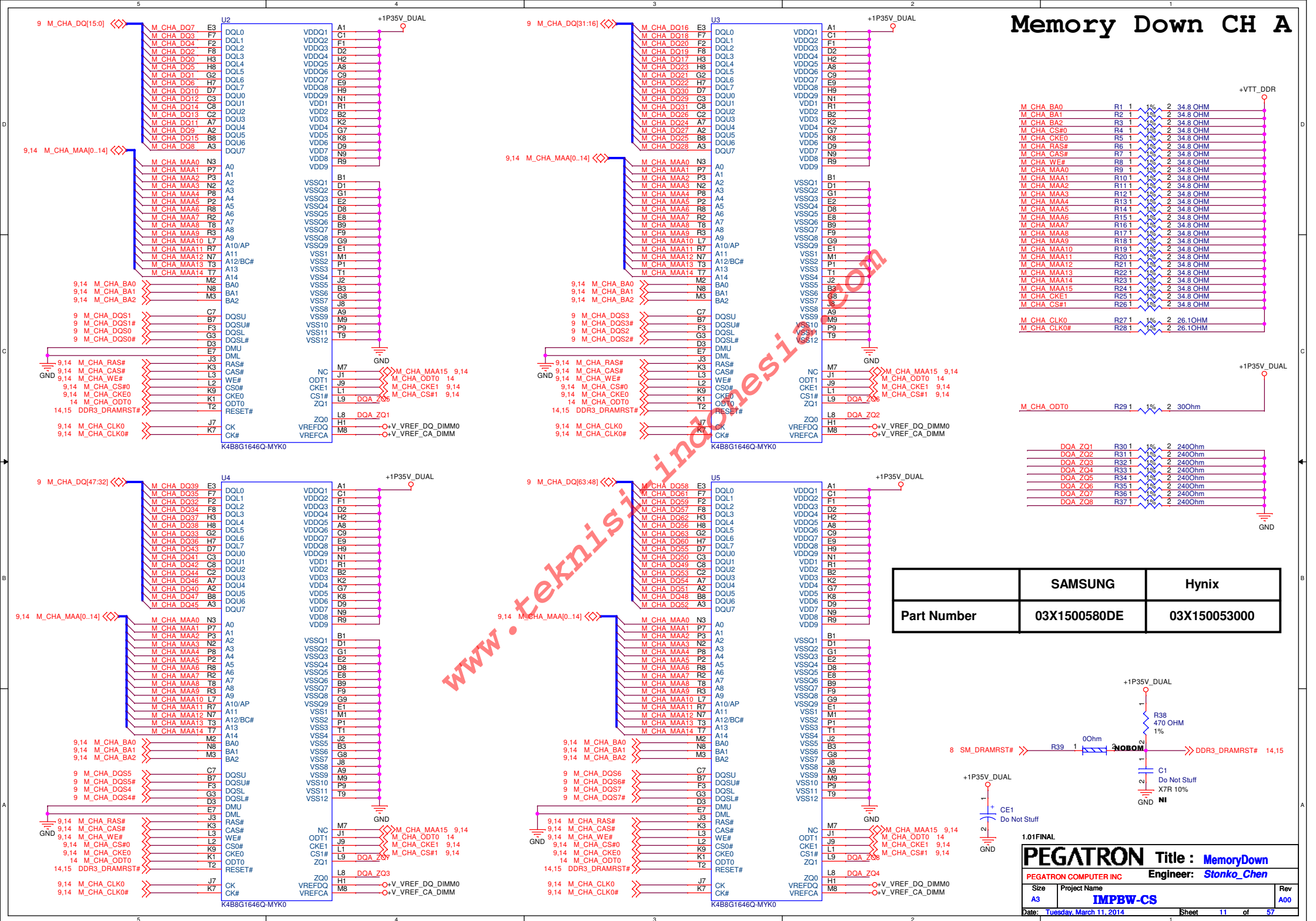


CPU XDP connector

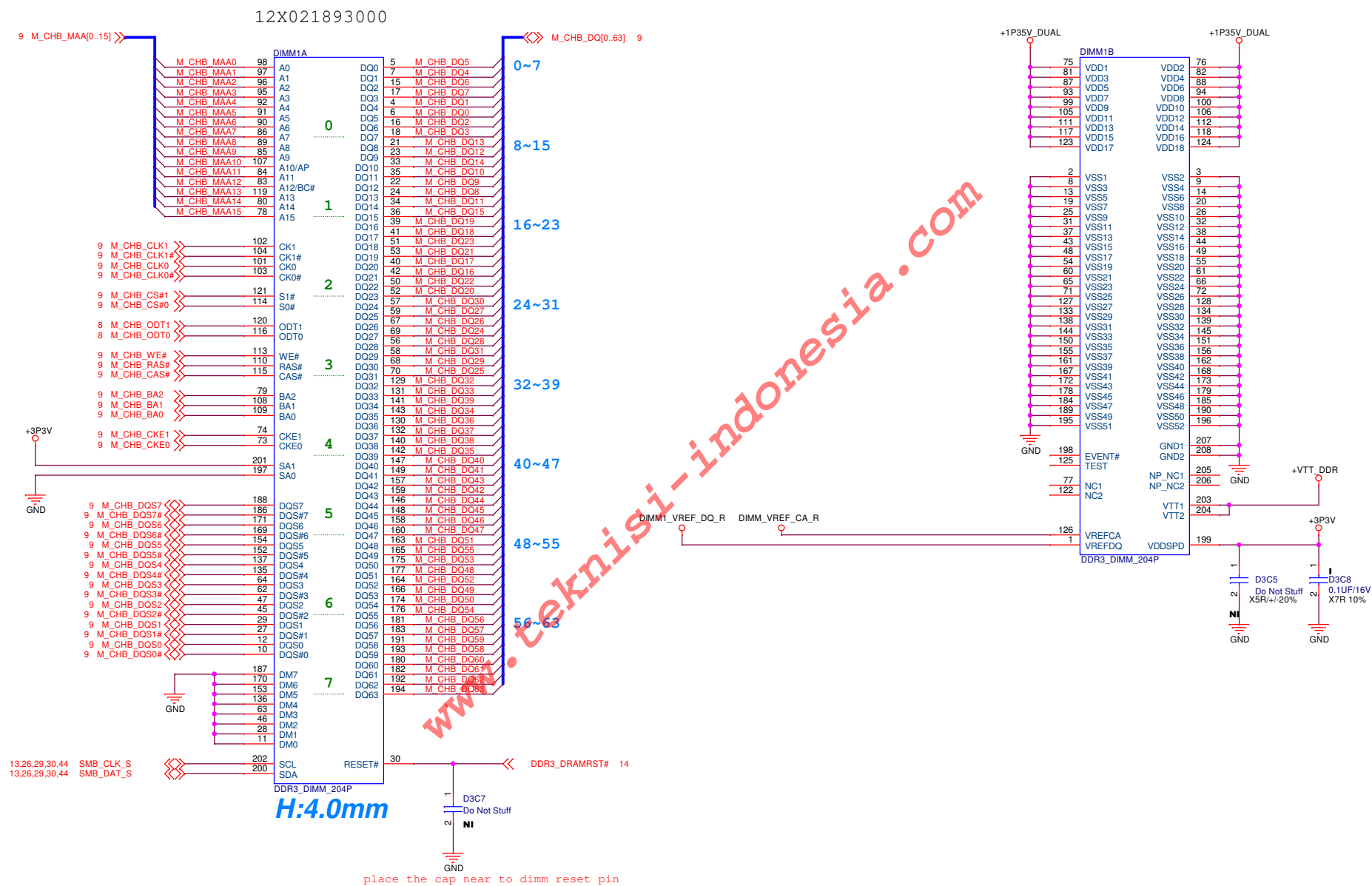
**Intel recommend (R1.0 on 9/10)
XDP pin 40, 42/HOOK4, 5 should be left Open,
unstuff R1006, R1007.**



Memory Down CH A



Memory SO-Dimm CH B



1.01FINAL

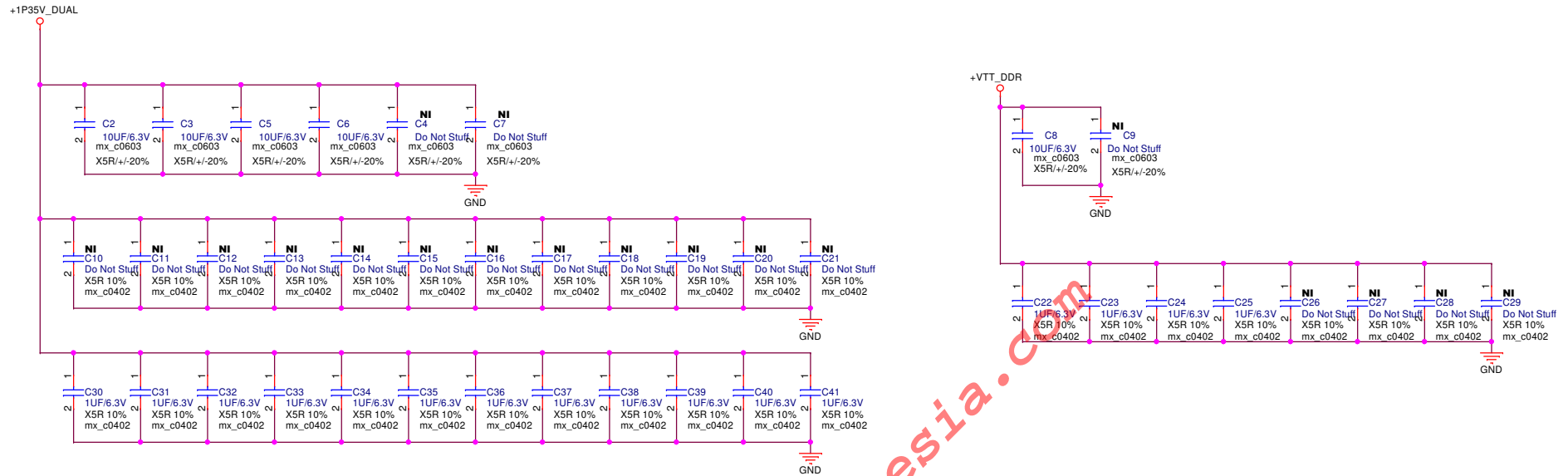
PEGATRON Title : **SO-DIMM**

PEGATRON COMPUTER INC Engineer: Stonko_Chen

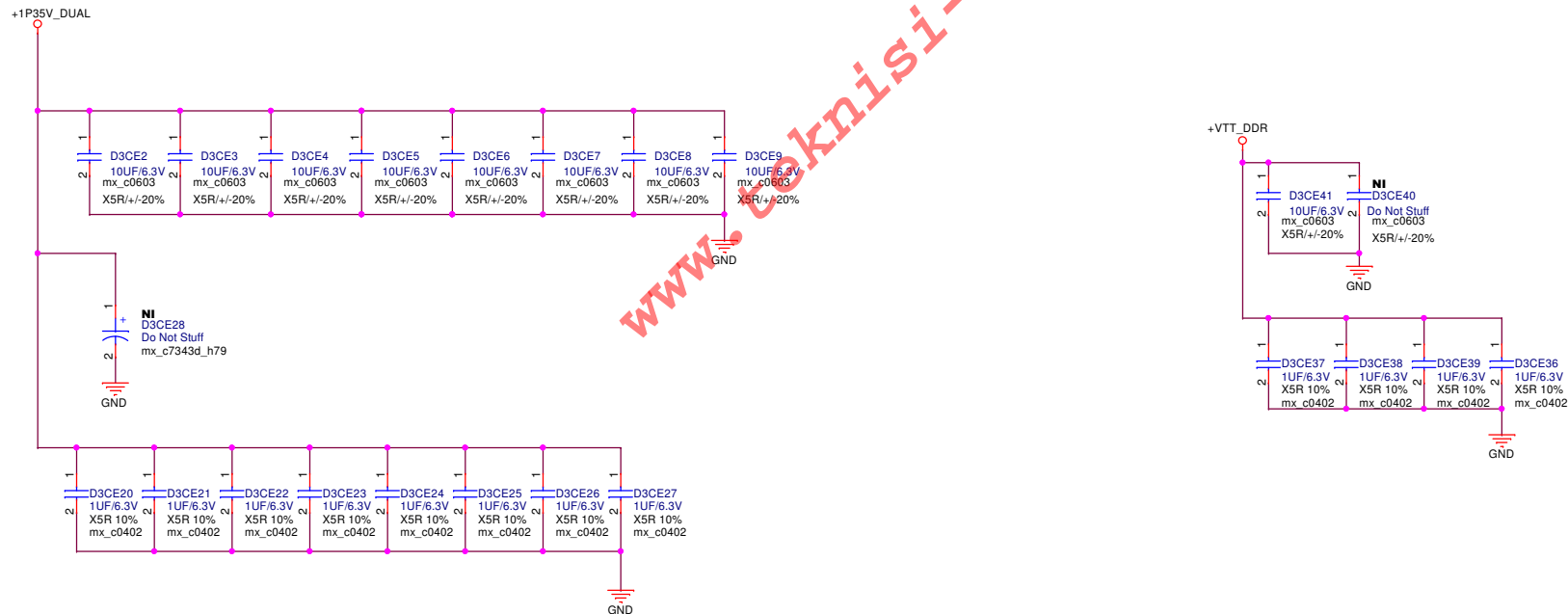
Size A3	Project Name IMPBW-CS	Rev A00
-------------------	---------------------------------	-------------------

Date: Tuesday, March 11, 2014 Sheet 12 of 57

DDR3L MEMORY DOWN CHANNEL-A PDBOM



DDR3L SODIMM CHANNEL-B PDBOM



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DDR3L-RS_Decoupling

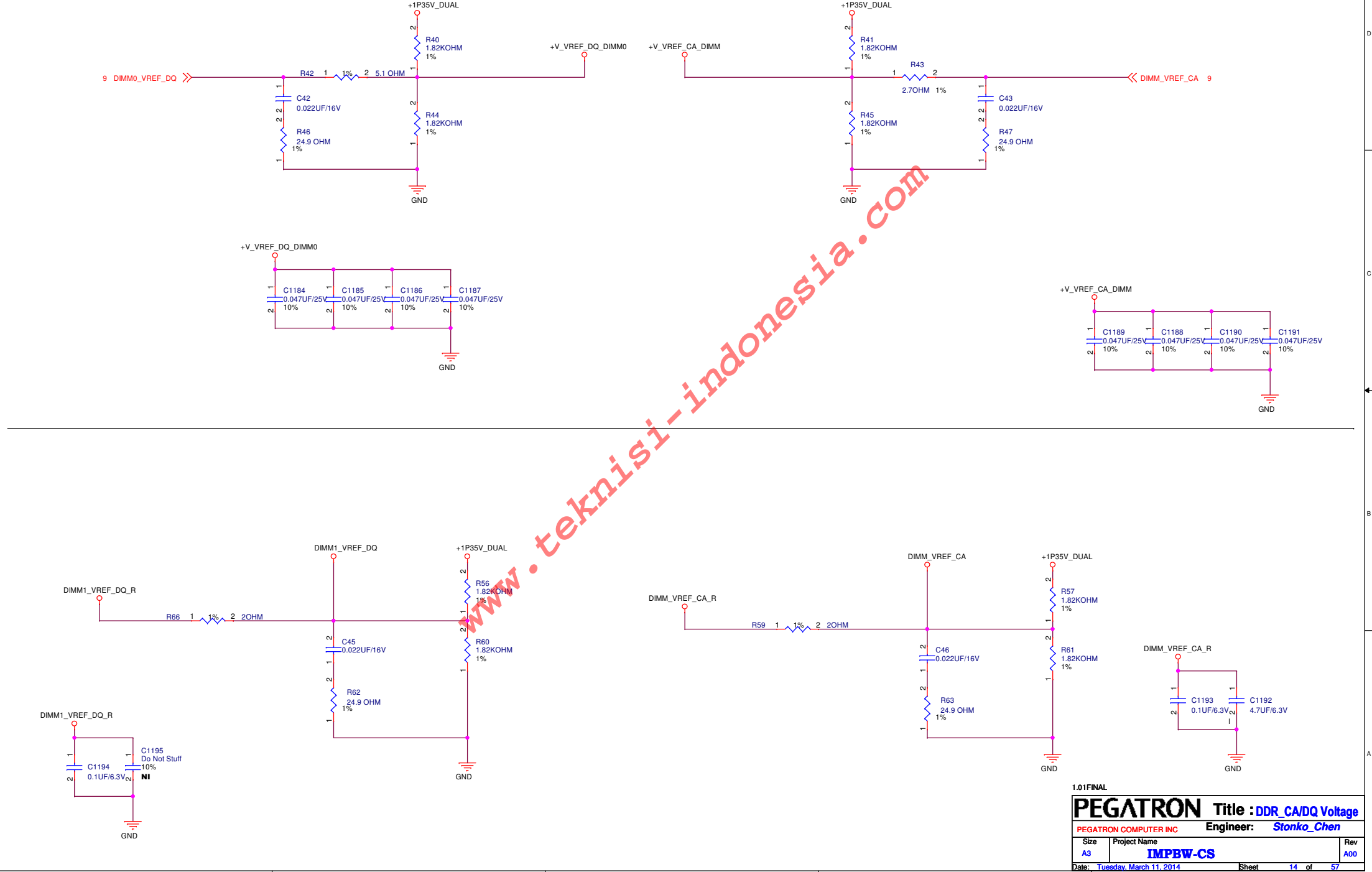
PEGATRON COMPUTER INC Engineer: *Stonko_Chen*

Size A3	Project Name IMPBW-CS	Rev A00
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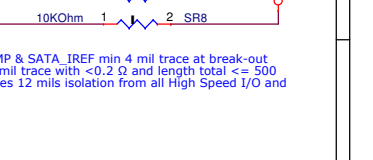
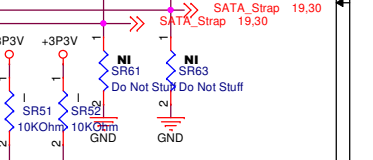
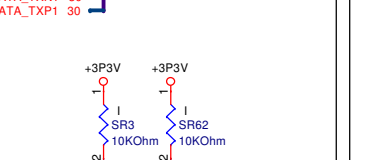
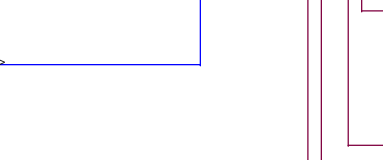
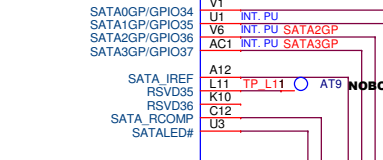
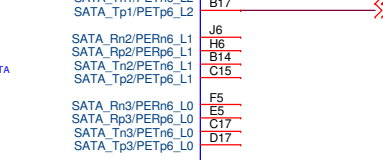
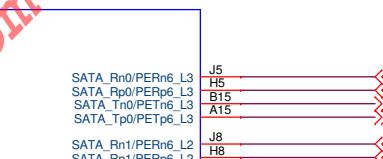
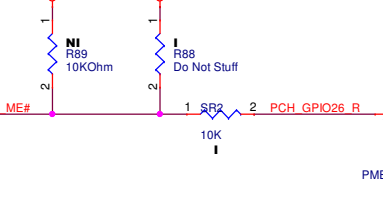
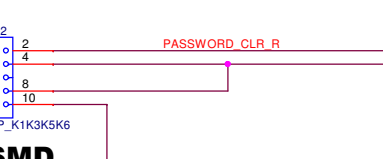
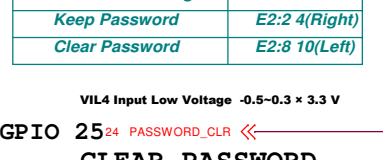
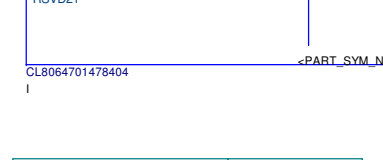
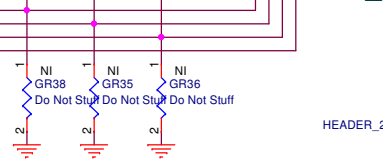
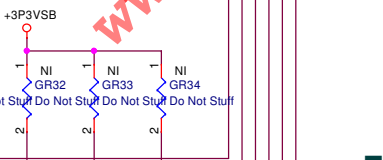
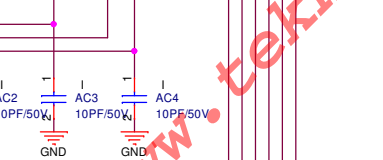
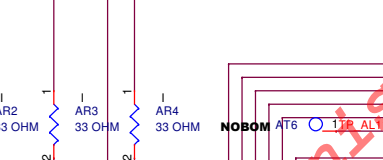
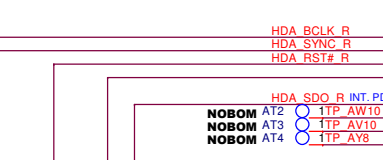
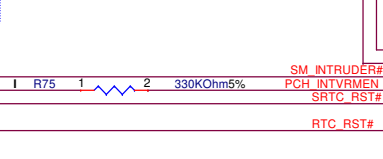
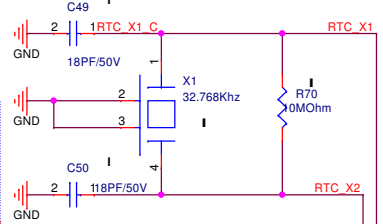
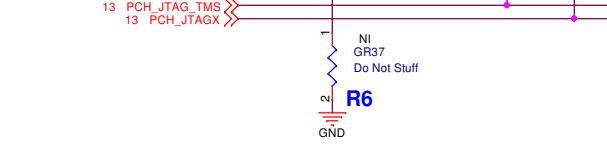
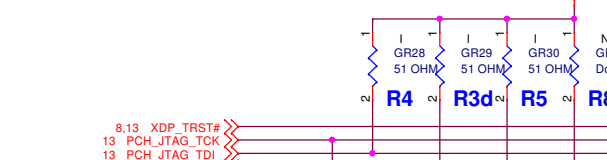
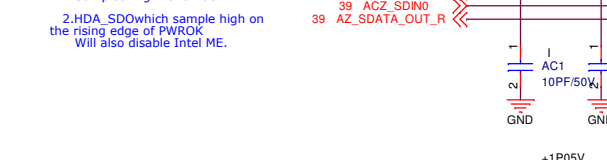
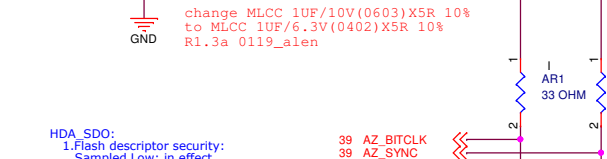
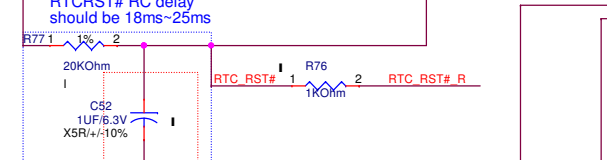
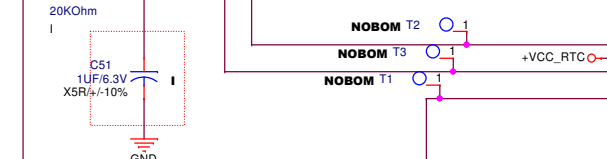
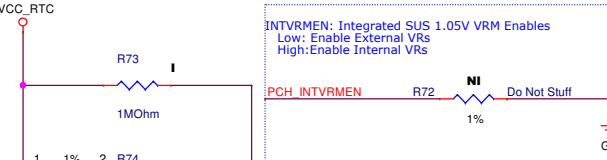
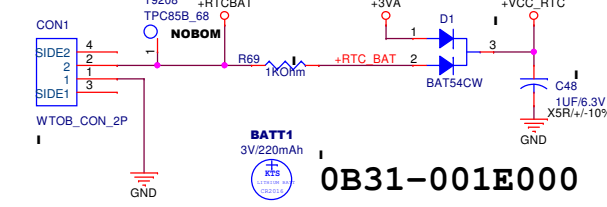
Date: Tuesday, March 11, 2014 Sheet 13 of 57

DDR3L Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



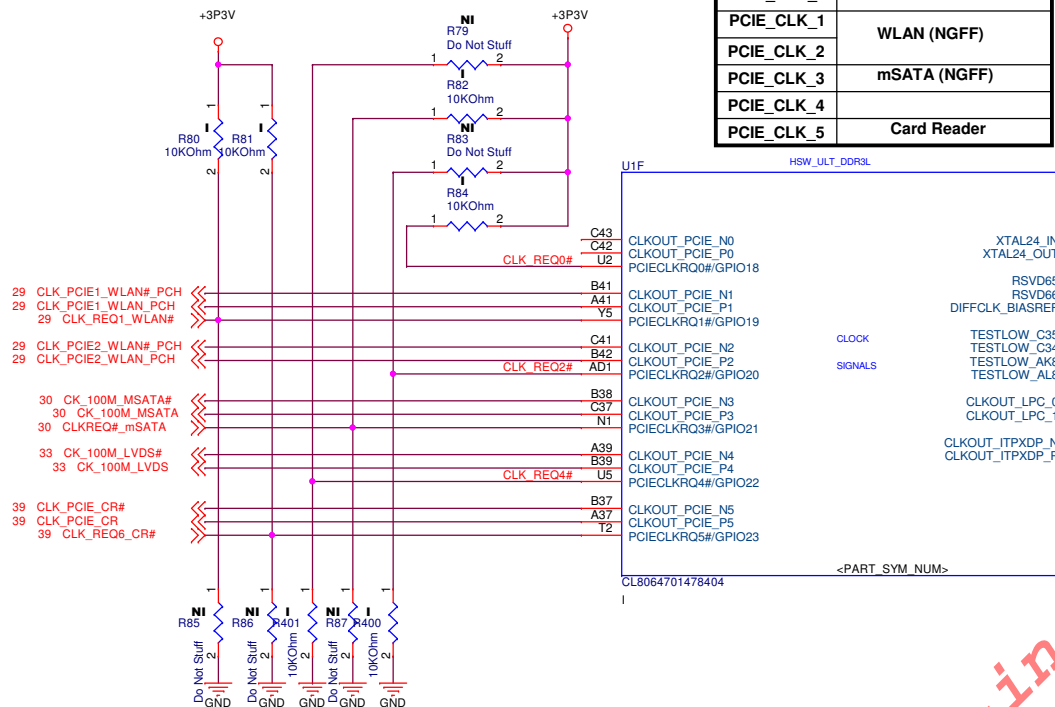
RTC battery 1217-001M000 替代料件



Connected to device.
Default : Clock free run. (PD 10K).
Reserver 10K PU for power saving purpose.

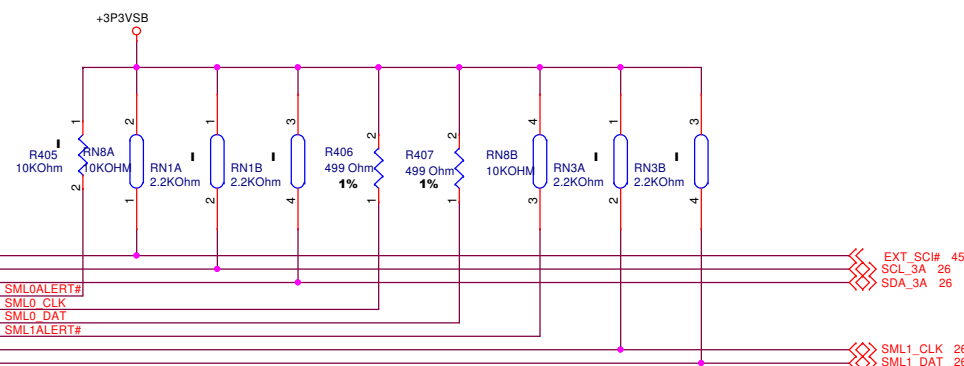
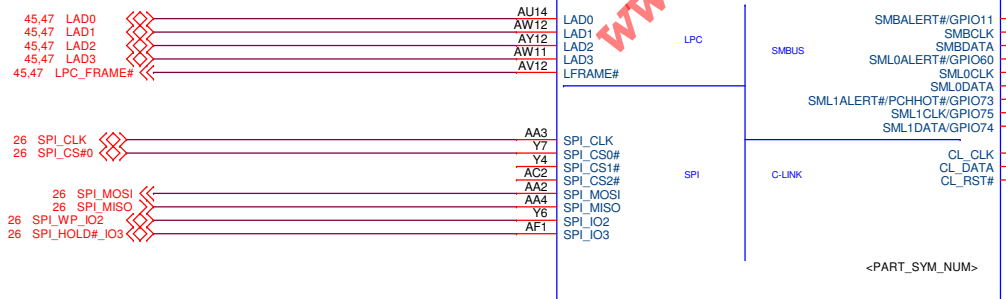
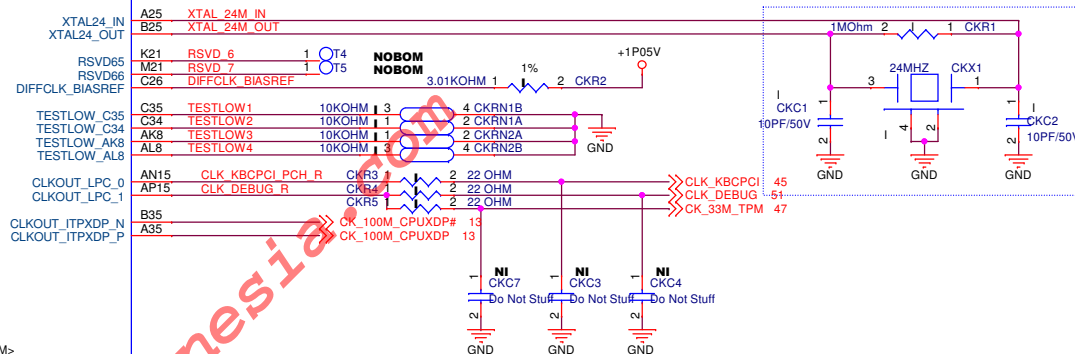
PCH CLKREQ Setting:
Not connected to device.
PCIECLKRQ[5:0]# are core well powered.

PCIE_CLK_0	
PCIE_CLK_1	WLAN (NGFF)
PCIE_CLK_2	
PCIE_CLK_3	mSATA (NGFF)
PCIE_CLK_4	
PCIE_CLK_5	Card Reader

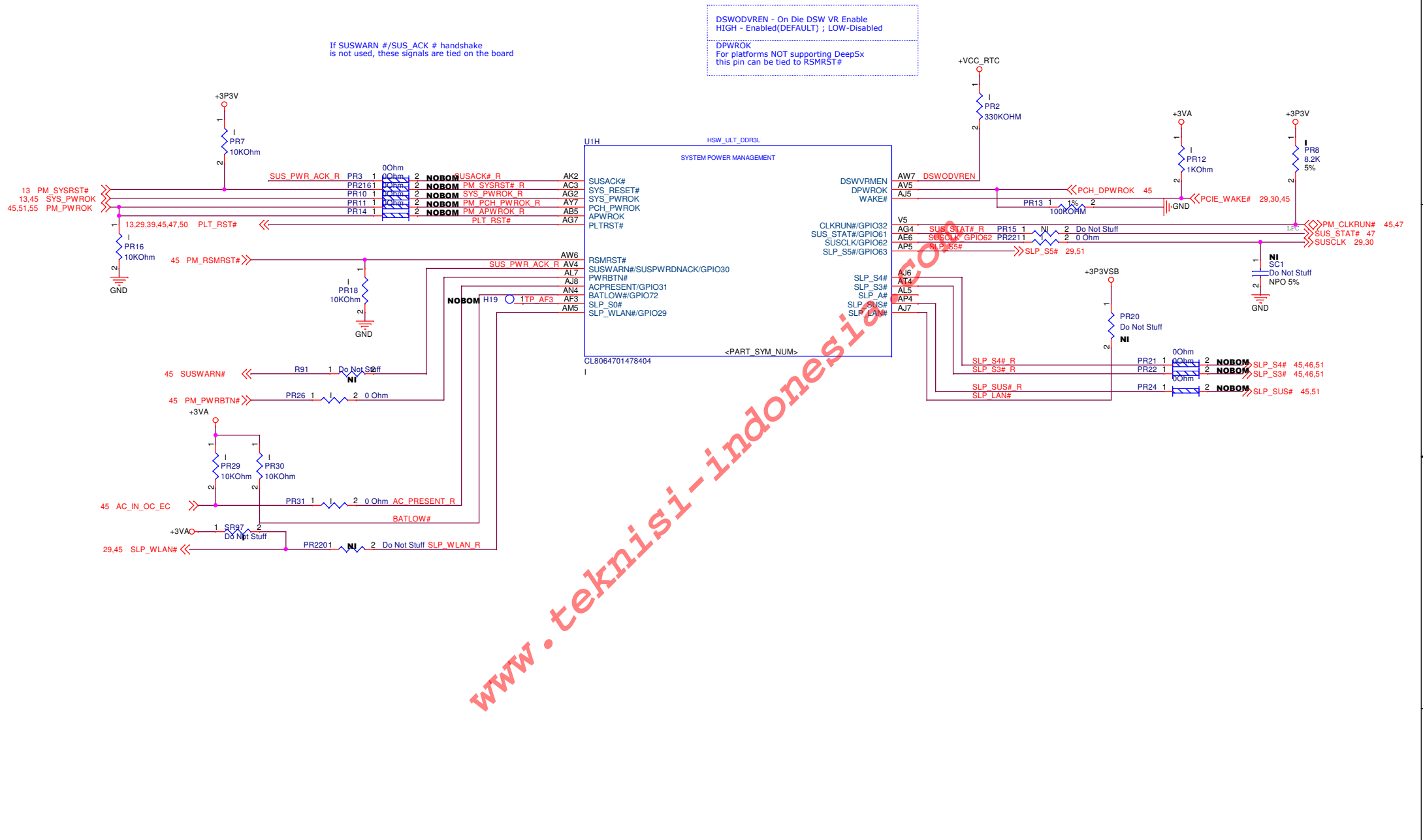


Swap XTAL_IN and XTAL_OUT, MOW 48999

24-MHz is required



1.01FINAL



If SUSWARN #/SUS_ACK # handshake is not used, these signals are tied on the board

DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled

DPWROK
For platforms NOT supporting DeepSx
this pin can be tied to RSMRST#

1.01FINAL

CARD READER

39 PCIE_RXN6_CR
39 PCIE_RXP6_CR
39 PCIE_TXN6_CR
39 PCIE_TXP6_CR

PCIE 1	
PCIE 2	
PCIE 3	
PCIE 4	NGFF Card (WLAN)
PCIE 5	Card Reader
PCIE 6	

WLAN

29 PCIE_RXN3_WLAN
29 PCIE_RXP3_WLAN
29 PCIE_TXN3_WLAN
29 PCIE_TXP3_WLAN

29 PCIE_RXN4_WLAN
29 PCIE_RXP4_WLAN
29 PCIE_TXN4_WLAN
29 PCIE_TXP4_WLAN

+1.05VS_AUSB3PLL

SR10

1

2

3.01KOHM

PCIE_RCOMP

NOBOM ST1

NOBOM ST2

TP E15 E15

TP E13 E13

A27

B27

U1K

HSW_ULT_DDR3L

F10 PERn5_L0
E10 PERp5_L0
C23 PETn5_L0
C22 PETp5_L0
F8 PERn5_L1
E8 PERp5_L1
B23 PETn5_L1
A23 PETp5_L1
H10 PERn5_L2
G10 PERp5_L2
B21 PETn5_L2
C21 PETp5_L2
E6 PERn5_L3
F6 PERp5_L3
B22 PETn5_L3
A21 PETp5_L3
G11 PERn3
F11 PERp3
C29 PETn3
B30 PETp3
F13 PERn4
G13 PERp4
B29 PETn4
A29 PETp4
G17 PERn1/USB3Rn3
F17 PERp1/USB3Rp3
C30 PETn1/USB3Tn3
C31 PETp1/USB3Tp3
F15 PERn2/USB3Rn4
G15 PERp2/USB3Rp4
B31 PETn2/USB3Tn4
A31 PETp2/USB3Tp4
RSVD26
RSVD27
PCIE_RCOMP
PCIE_IREF

PCIE

USB

<PART_SYM_NUM>

CL8064701478404

AN8 USB_PN0 39
AM8 USB_PP0 39
AR7 USB_PN1 39
AT7 USB_PP1 39
AR8 USB_PN2 38
AP8 USB_PP2 38
AR10 USB_PN3 37
AT10 USB_PP3 37
AM15 USB_PN4 39
AL15 USB_PP4 39
AM13 USB_PN5 42
AN13 USB_PP5 42
AP11 USB_PN6 29
AN11 USB_PP6 29
AR13 USB_PN7 30
AP13 USB_PP7 30
Q20 USB3_RXN0 36
H20 USB3_RXP0 36
C33 USB3_TXN0 36
B34 USB3_TXP0 36
E18 USB3_RXN1 36
F18 USB3_RXP1 36
B33 USB3_TXN1 36
A33 USB3_TXP1 36

USBRBIAS#
USBRBIAS
RSVD50
RSVD51

OC0#/GPIO40
OC1#/GPIO41
OC2#/GPIO42
OC3#/GPIO43

USB2.0 port - Combo with USB3.0-R
USB2.0 port - Combo with USB3.0-L
Camera
Touch Screen
USB2.0 port RF
Sensor Hub
WiFi
mSATA

USB3.0

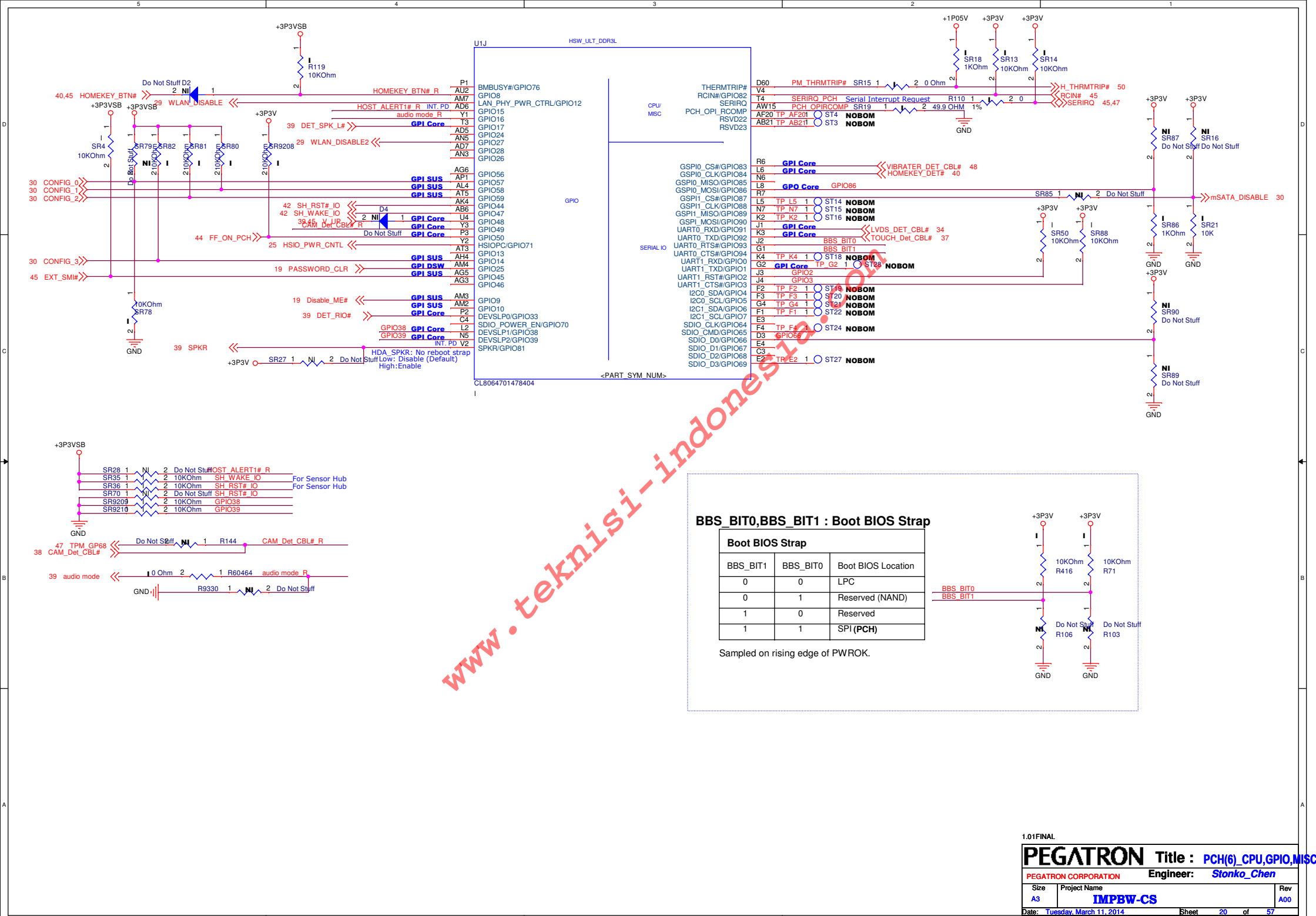
USB3.0

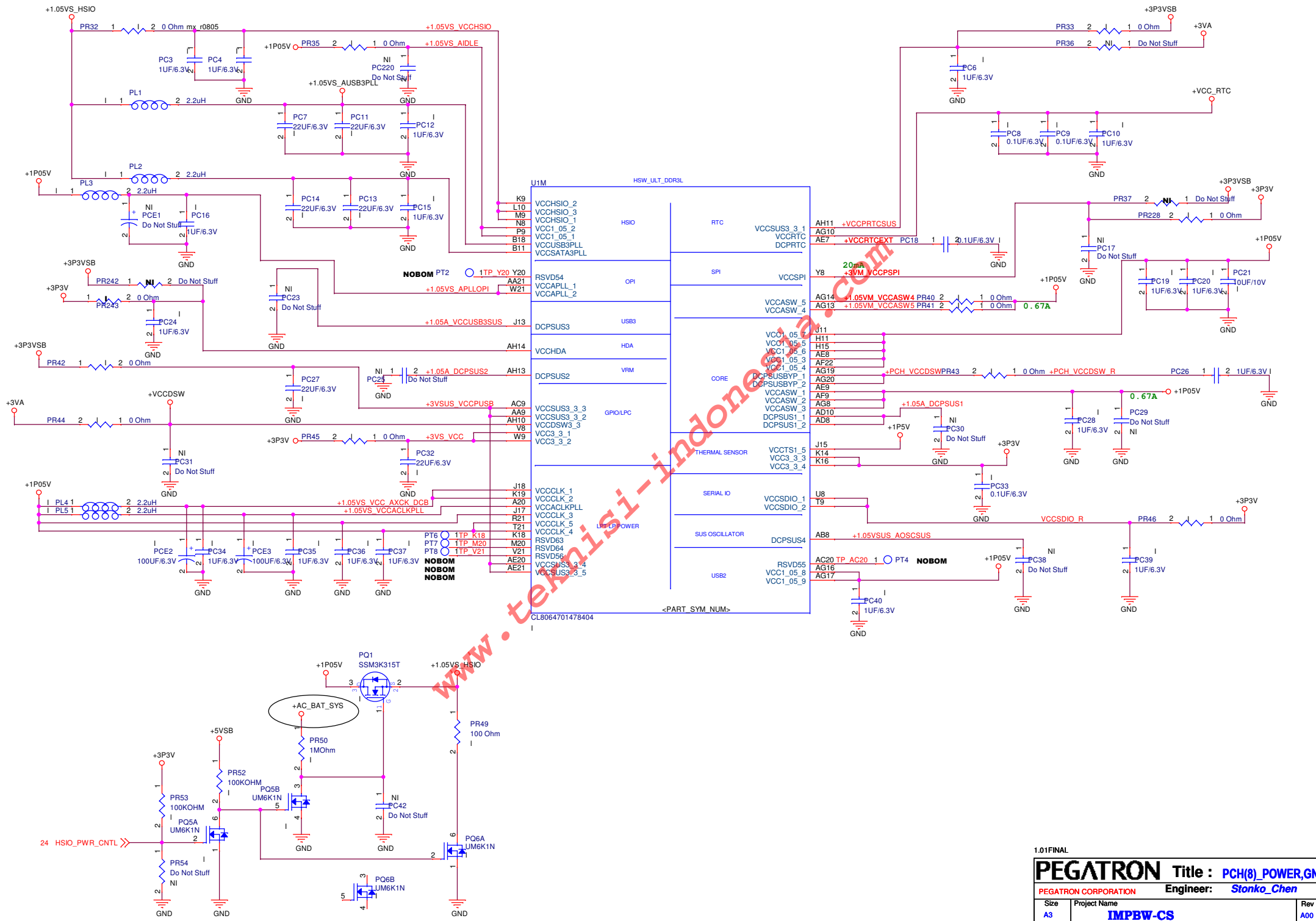
USBCOMP (R2403): TIE TRACES TOGETHER CLOSE
TO PINS, WITH LENGTH NO
LONGER THAN 450 MILS TO RESISTOR

AJ10 USB_BIAS R108 1 1% 22.6 OHM
AN10
AM10
GND

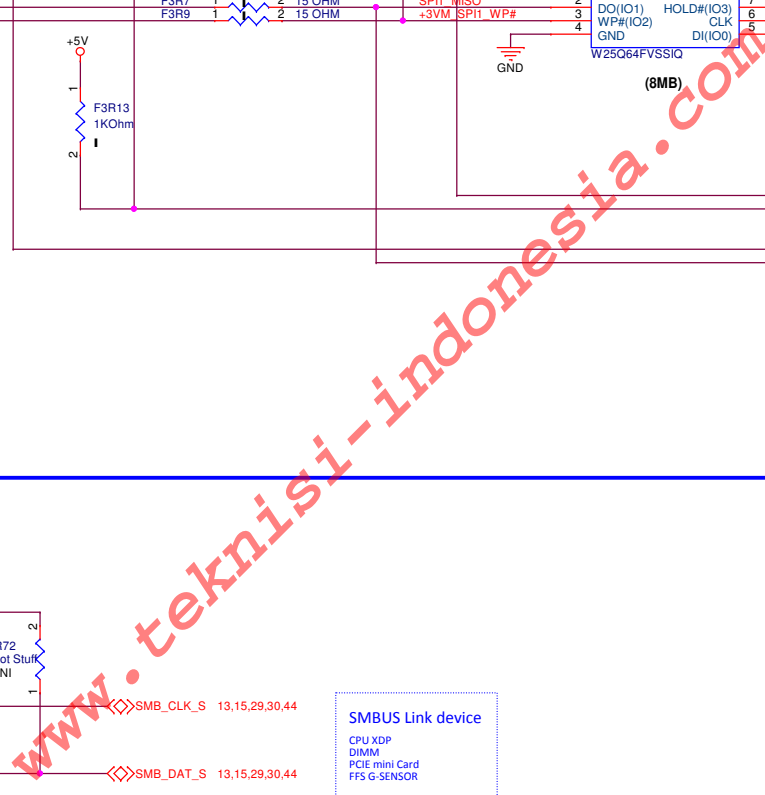
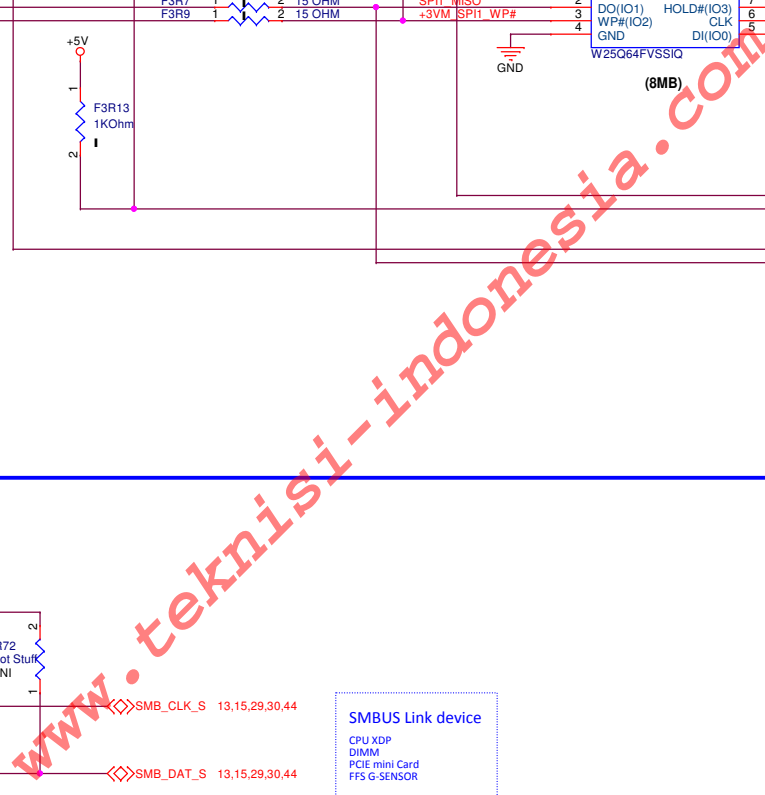
+3P3VSB
R109
10KOhm

1.01FINAL





The diagram shows a W25Q64FVSSIQ memory chip connected to an NI-7201 module. The chip is connected to a +5V supply and GND. The NI-7201 module is connected to the chip via an SMBUS link. The NI-7201 module is also connected to a +5V supply and GND. The NI-7201 module is labeled 'NI-7201' and '13,15,29,30,44'.



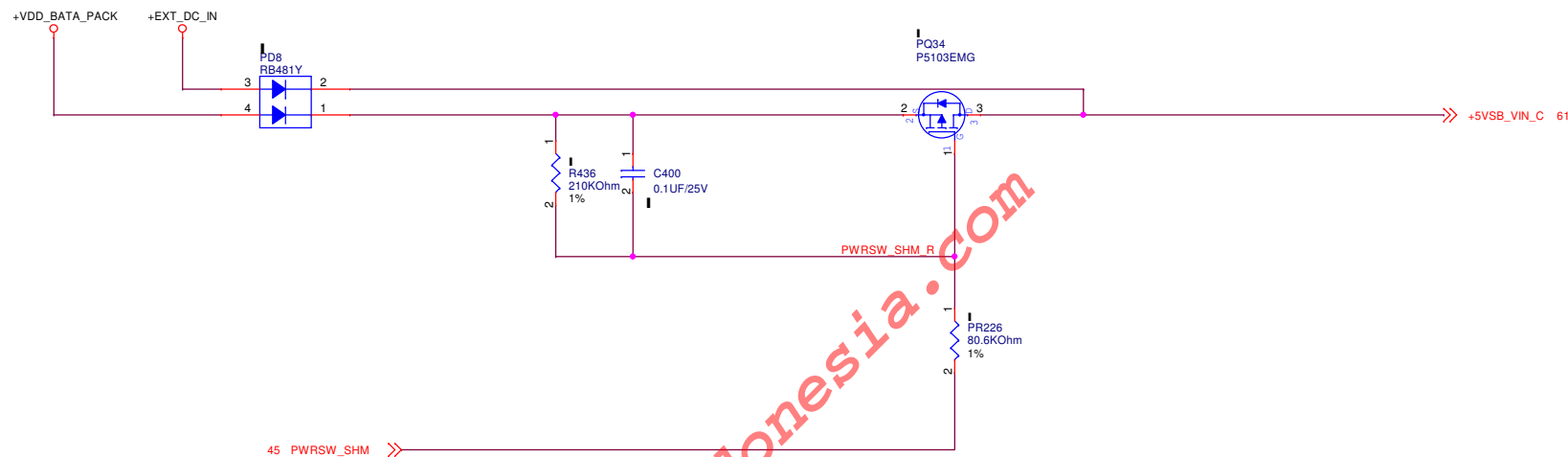
W25Q64FVSSIQ (8MB)

Pin	Function
1	DO(I/O1)
2	WP#(IO2)
3	GND
4	HOLD#(IO3)
5	CLK
6	DI(IO0)

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PEGATRON		Title : PCH(9)_SPI,SMB	
PEGATRON CORPORATION		Engineer: <i>Stonko_Chen</i>	
Size A3	Project Name IMPBW-CS	Rev A00	
Date: Tuesday, March 11, 2014	Sheet 22	of 57	

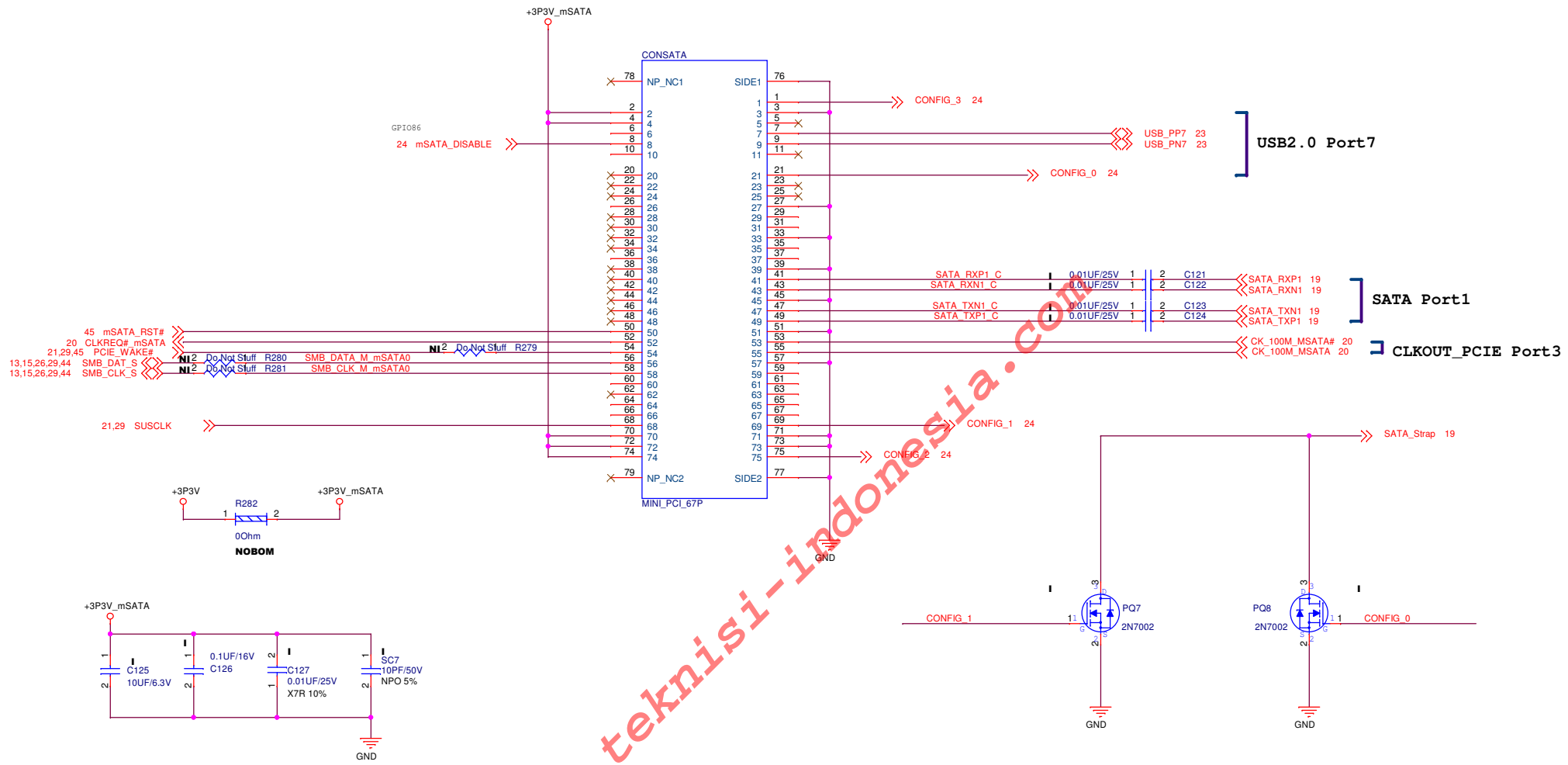
PEGATRON		Title : PCH(9)_SPI,SMB	
PEGATRON CORPORATION		Engineer: <i>Stonko_Chen</i>	
Size A3	Project Name IMPBW-CS	Rev A00	
Date: Tuesday, March 11, 2014	Sheet 22	of 57	

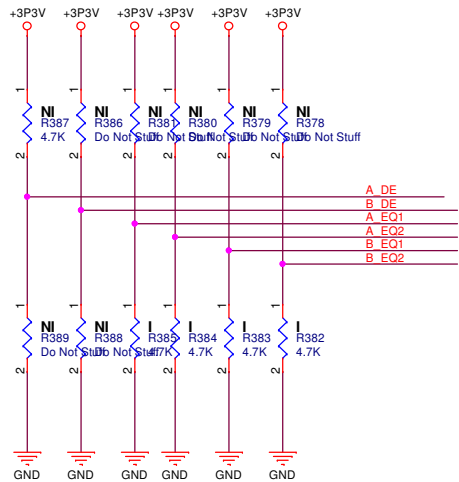
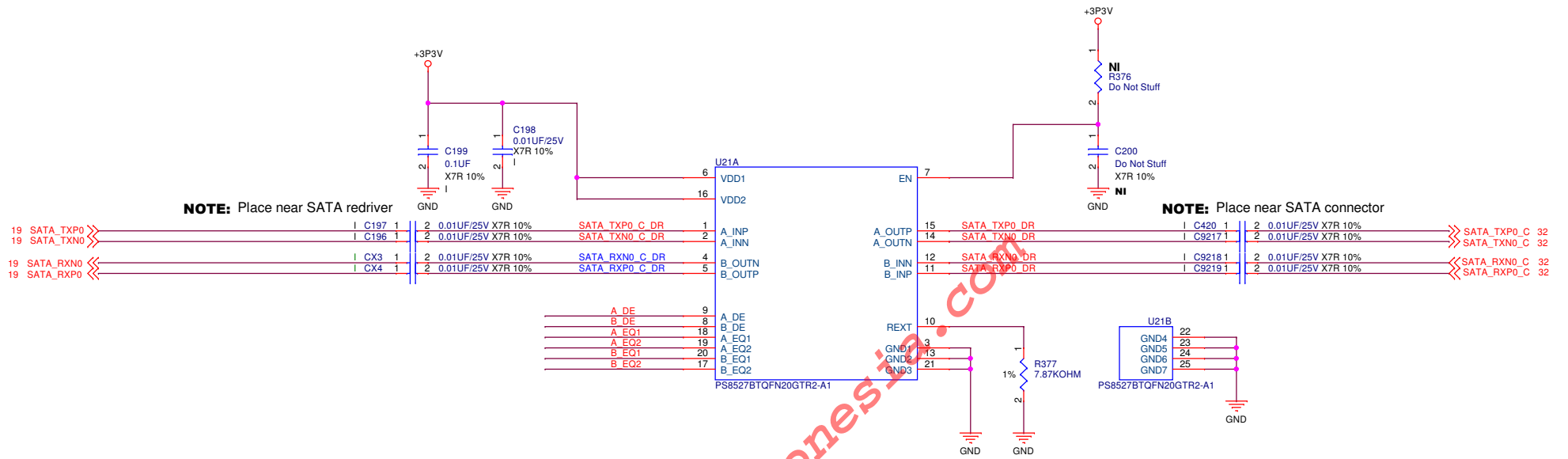


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1.01FINAL

PEGATRON		Title : shippingmode	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS	Rev A00	
Date: Tuesday, March 11, 2014		Sheet 23 of 57	

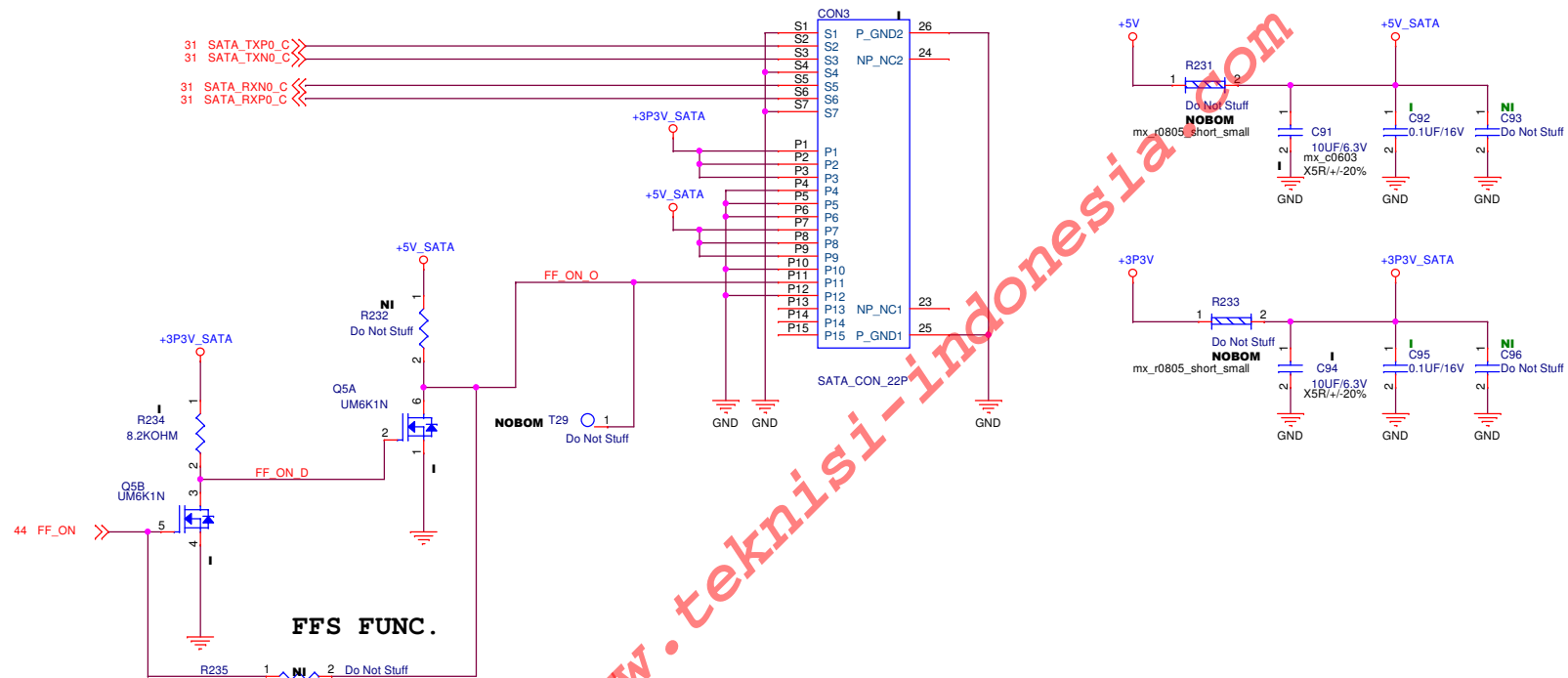


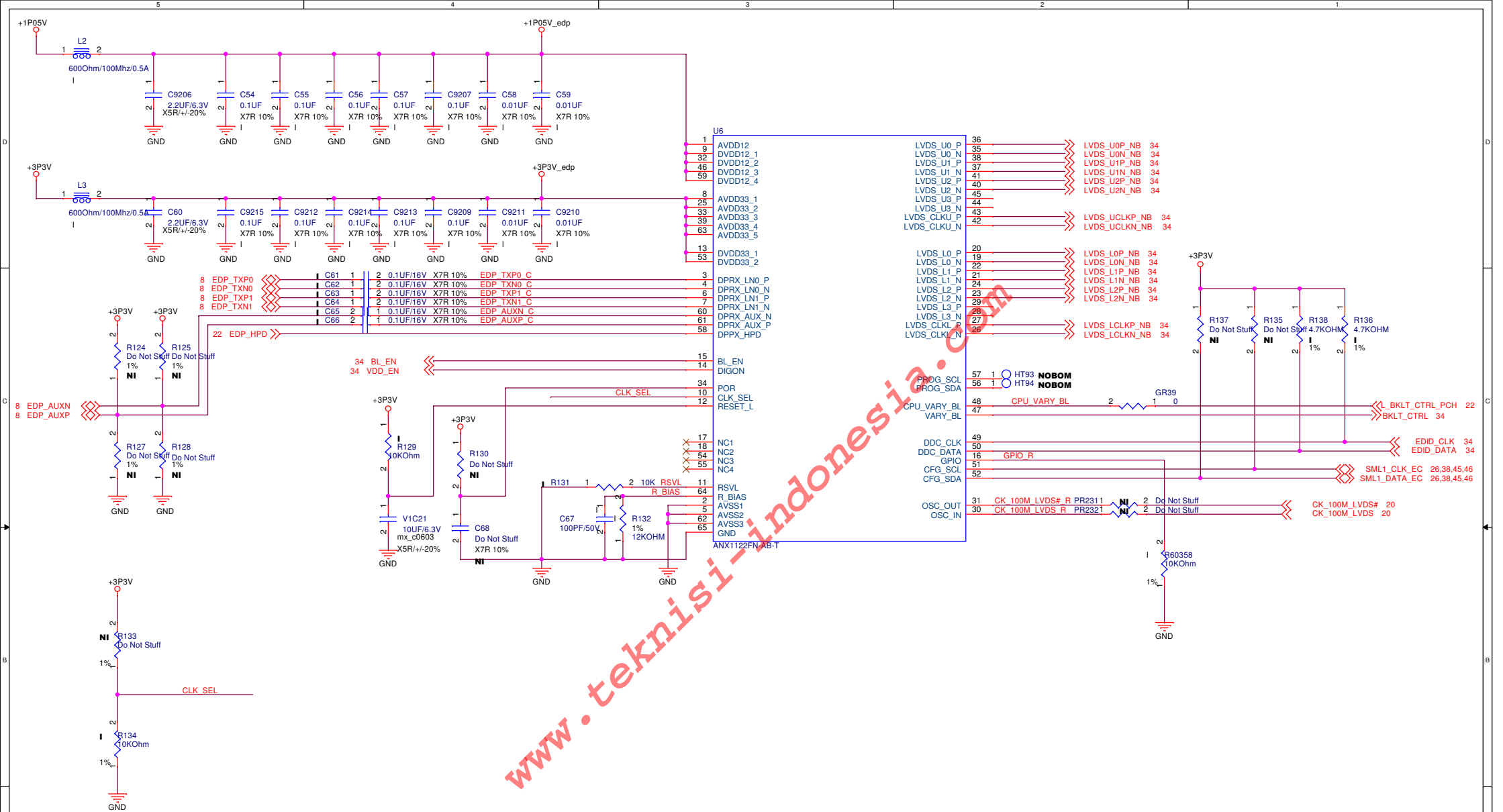


A/B_EQ2	A/B_EQ1	EQ for channel loss
L	M	2.4dB
L	L	7.4dB
L	H	14.4dB
M	M	12.2dB(default)
M	L	9.4dB
M	H	13.3dB
H	M	6.2dB
H	L	11.2dB
H	H	5dB

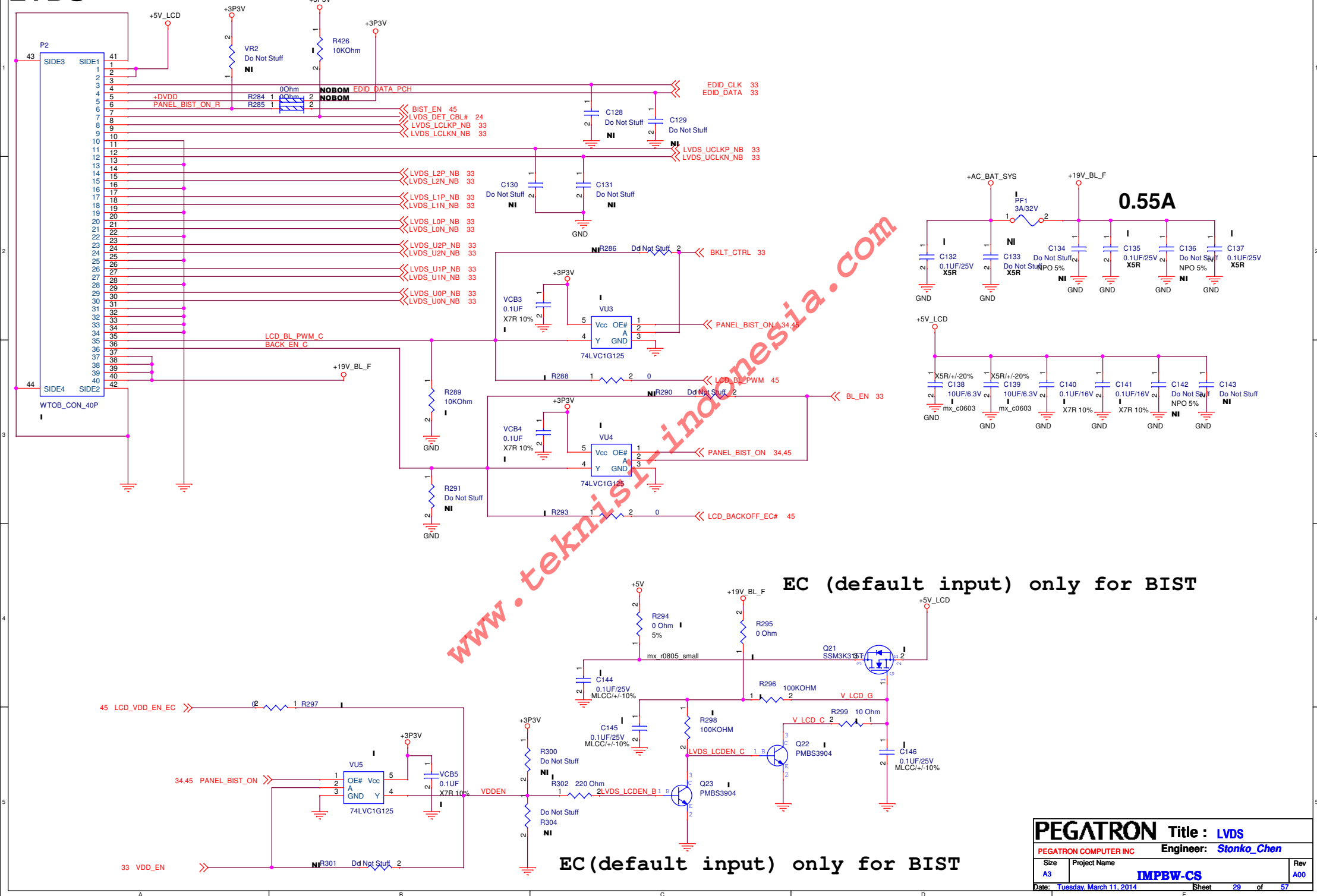
A/B_DE	De_Emphasis
M	-3.5dB(Default)
L	0dB
H	-1.5dB

SATA HDD





LVDS



USB 3.0 redriver

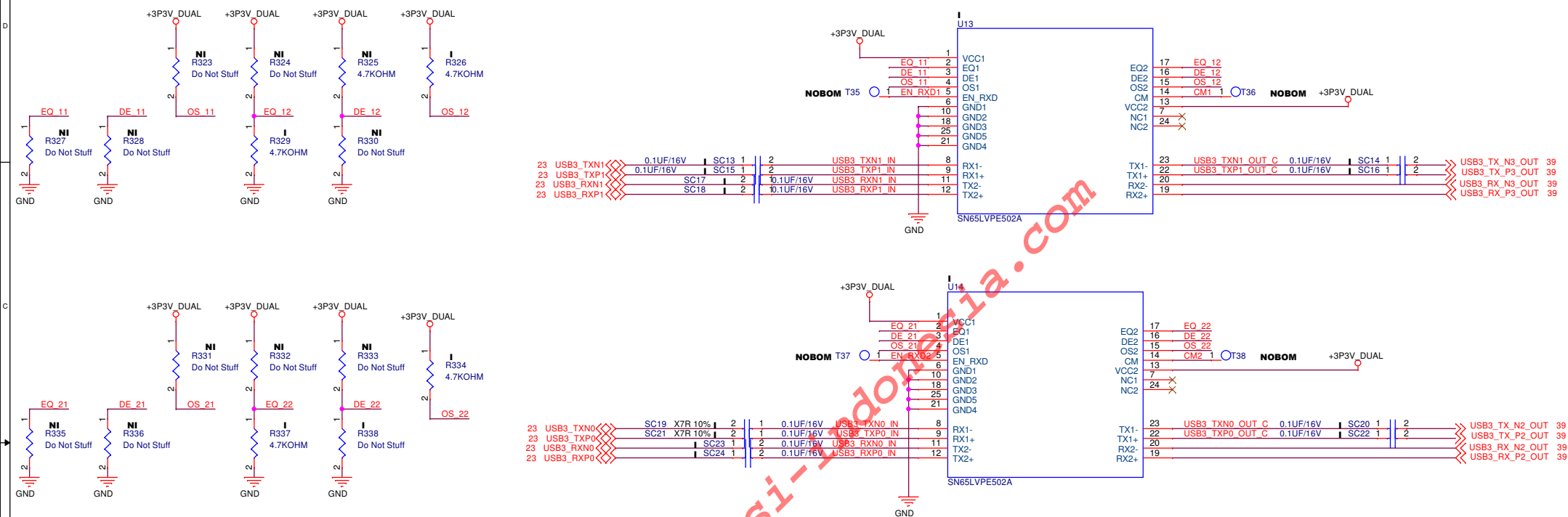
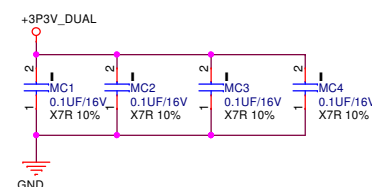
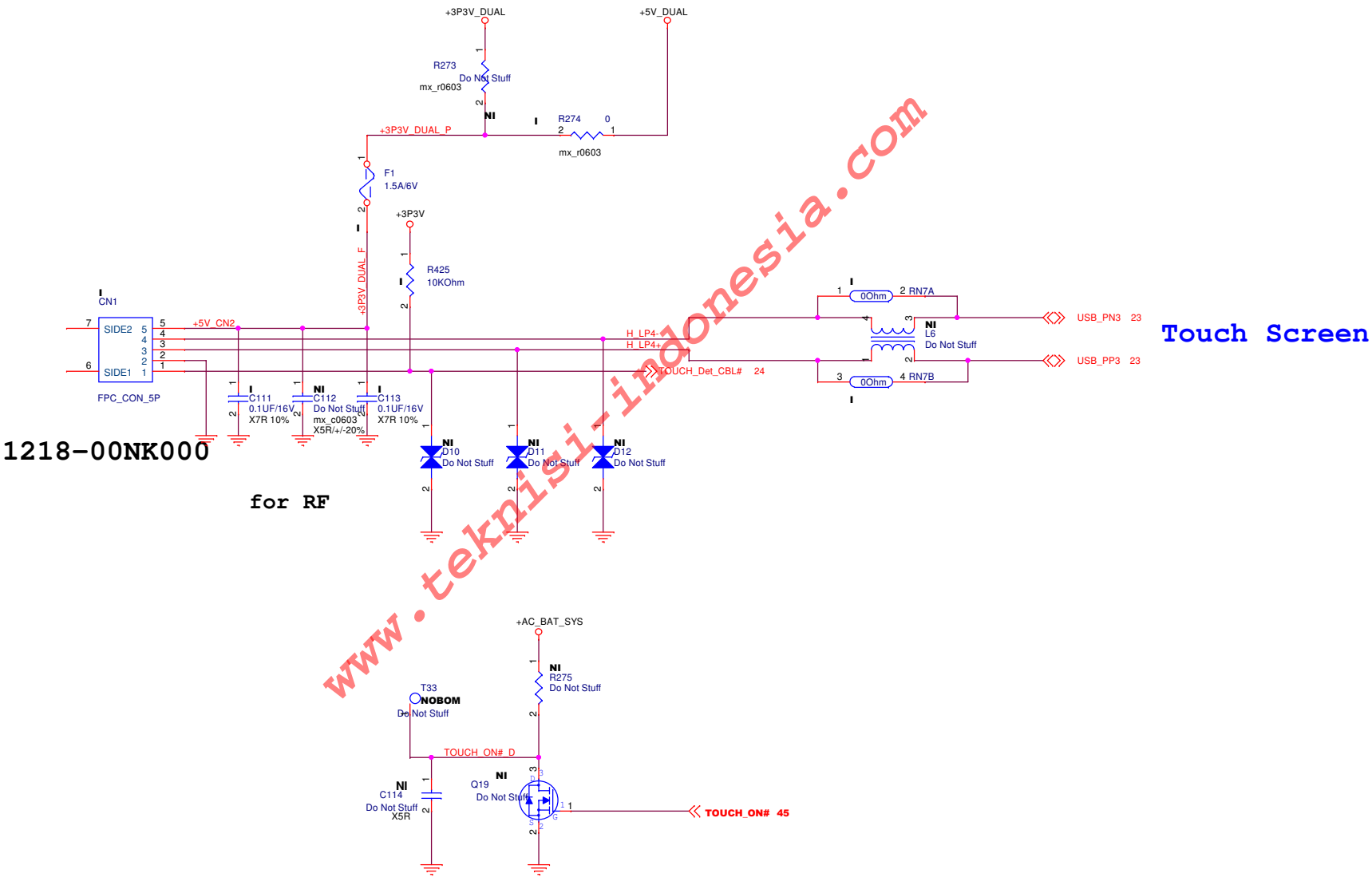


Table 2. Signal Control Pin Setting

OUTPUT SWING AND EQ CONTROL (at 2.5 GHz)			
OSx ⁽¹⁾	TRANSITION BIT AMPLITUDE (TYP mVpp)	EQx ⁽¹⁾	EQUALIZATION (dB)
NC (default)	1042	NC (default)	0
0	908	0	7
1	1127	1	15
OUTPUT DE CONTROL (at 2.5 GHz)			
DEx ⁽¹⁾	OSx ⁽¹⁾ = NC	OSx ⁽¹⁾ = 0	OSx ⁽¹⁾ = 1
NC (default)	0 dB	0 dB	0 dB
0	-3.5 dB	-2.2 dB	-4.4 dB
1	-6.0 dB	-5.2 dB	-6.0 dB
CONTROL PINS SETTINGS			
EN_RXD	DEVICE FUNCTION	CM	DEVICE FUNCTION
1 (default)	Normal Operation	0 (default)	Normal Operation
0	Sleep Mode	1	Compliance Test Mode



TOUCH

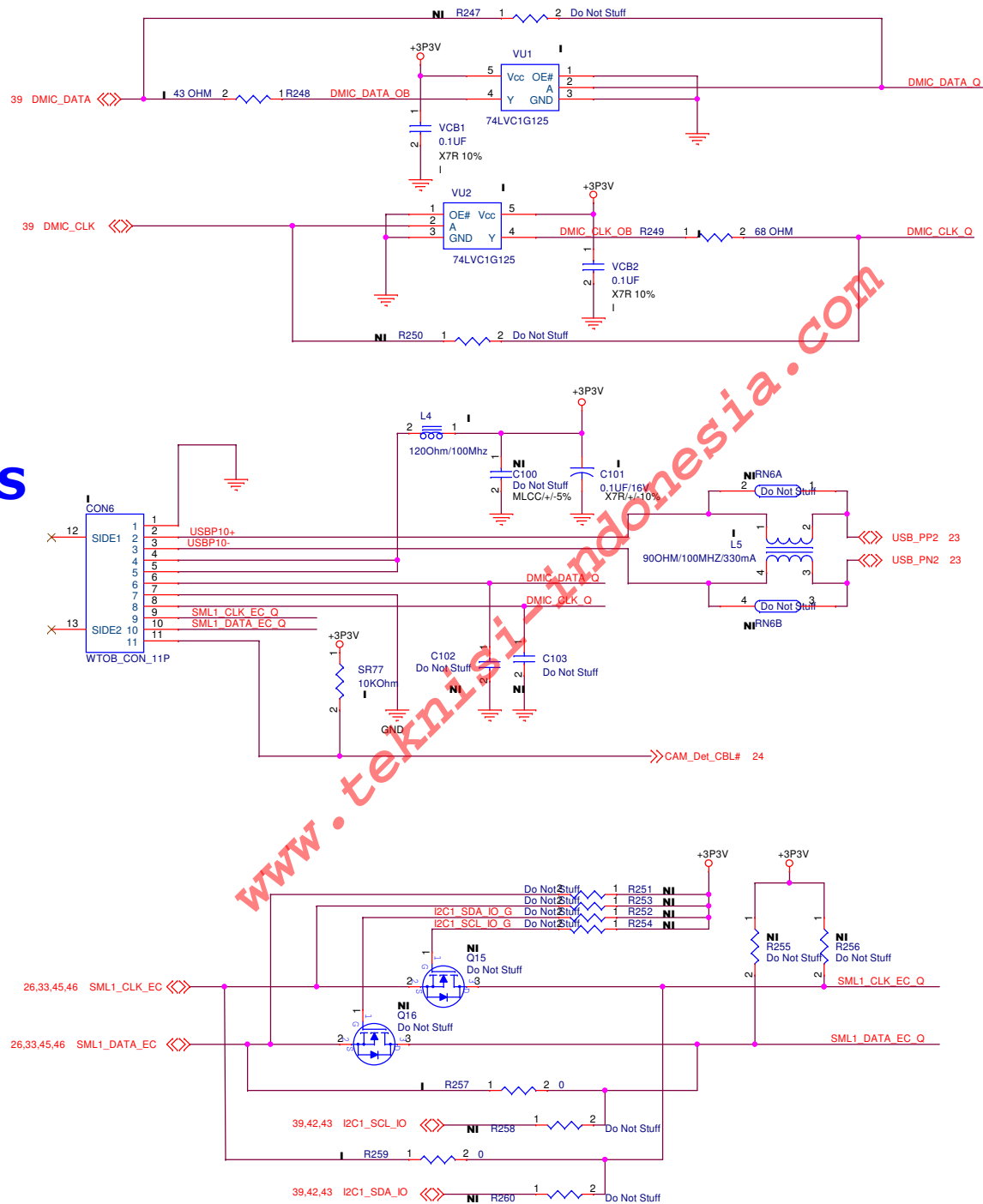


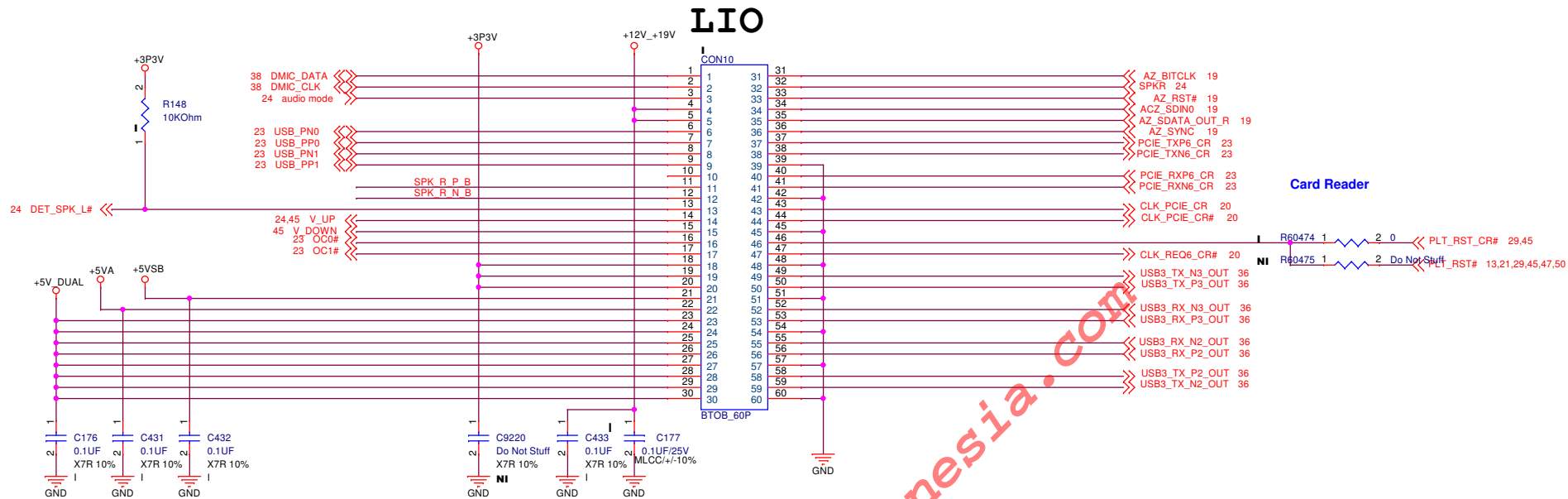
Camera Module & DMIC & ALS

Digital MIC

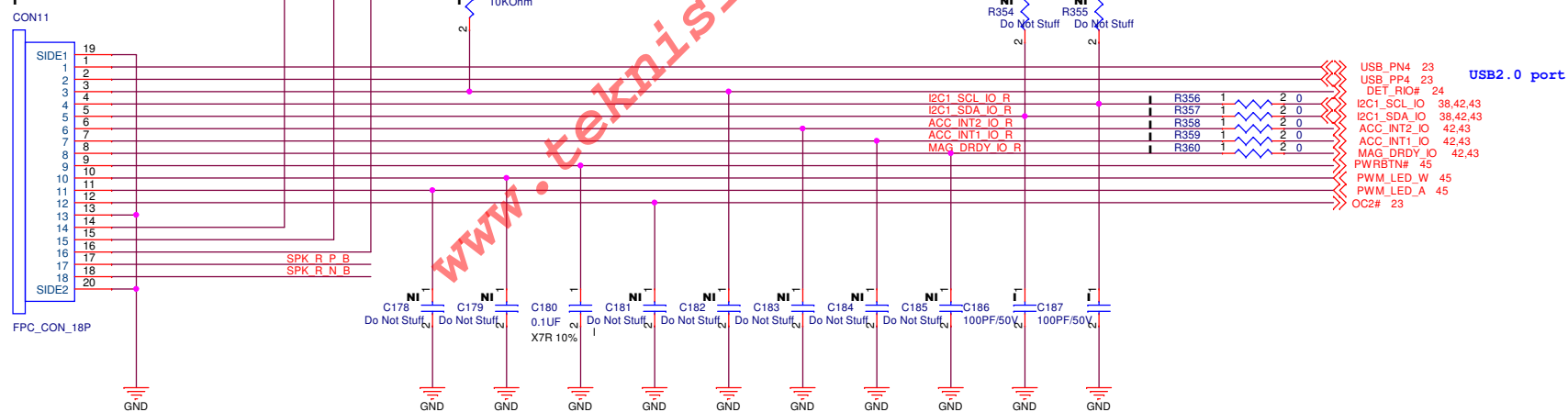
CAMERA

ALS



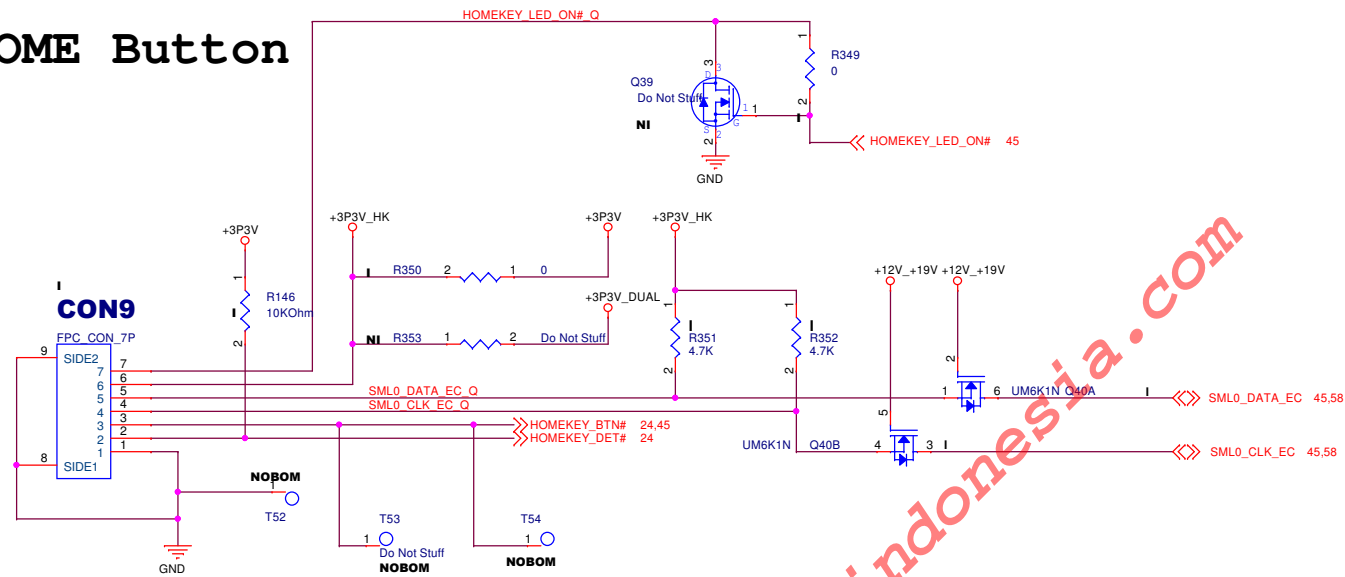


RIO



1.01FINAL

The diagram illustrates the power and signal architecture of the NOBOM board. It features a +3P3V_DUAL voltage regulator and a +3P3V_HK fuse. A +12V_-+19V regulator is also shown. Resistors R351 (4.7K) and R352 (4.7K) are connected to the regulators. Transistors UM6K1N and Q40B are used for signal processing. Signal lines for HOMEKEY_BTN# (pin 24) and HOMEKEY_DET# (pin 45) are connected to the board. A T54 component is also present.



PEGATRON		Title : <i>Homekey_connector</i>	
PEGATRON COMPUTER INC		Engineer: <i>Stonko_Chen</i>	
Size A3	Project Name IMPBW-CS	Rev A00	
Date: <i>Tuesday, March 11, 2014</i>		Sheet	34 of 57

Sensor Hub - IT8350E

Layout Notice

1. For the ADC layout notice circuits,
 - a) Keep the trace away from Power, fast data bus, and CRTs. Especially PWM DC-DC control.
 - b) Isolate Analog and Digital ground plane.

2. For all power plane,

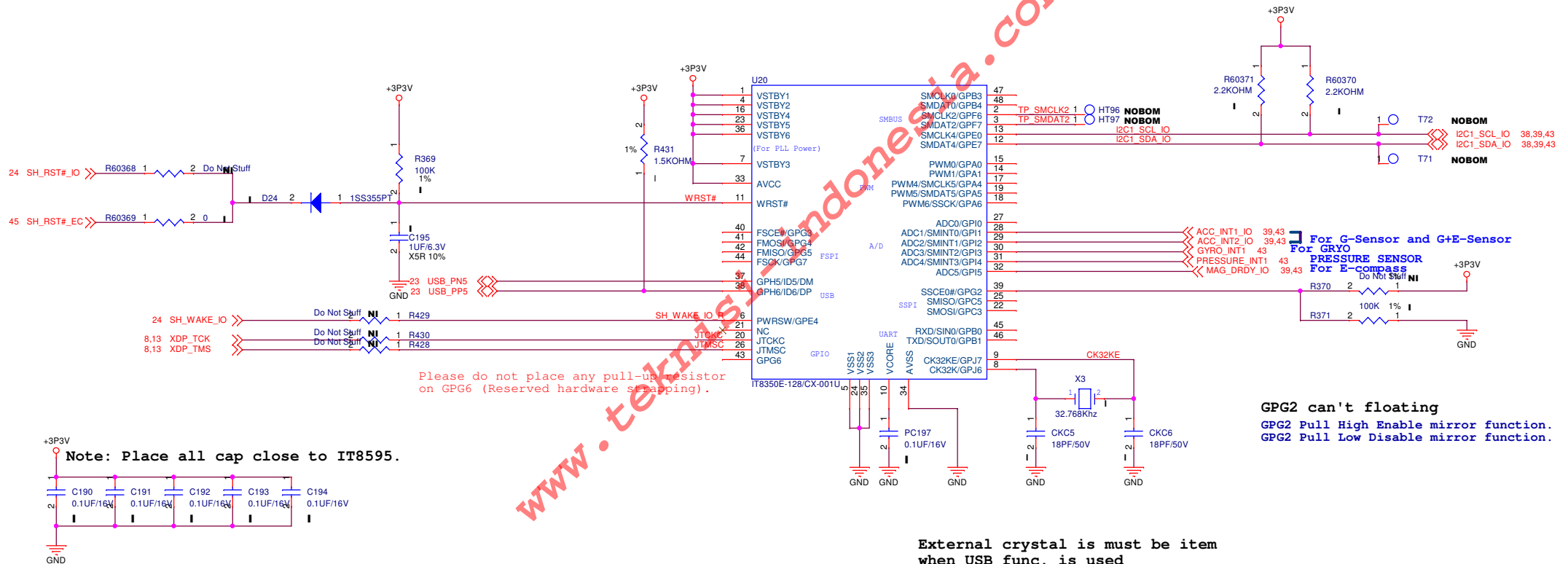
*Recommended net "VSTBY" minimum trace width 12mils.

Note 1 :

Since all GPIO belong to VSTBY power domain

Note 2 :

- (1) Each input pin should be driven or pulled.
- (2) Each output-drain output pin should be pulled.

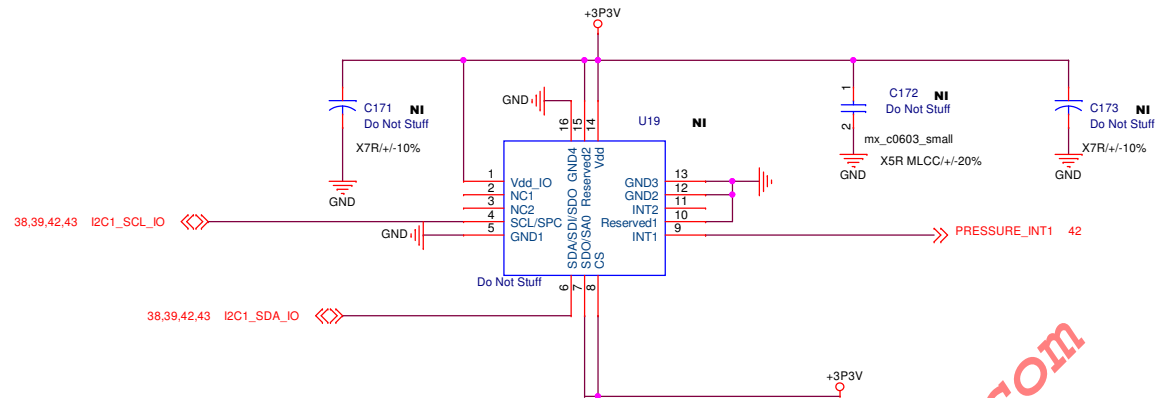


External crystal is must be item when USB func. is used

32.768kHz clock lines:(for USB must use external crystal)

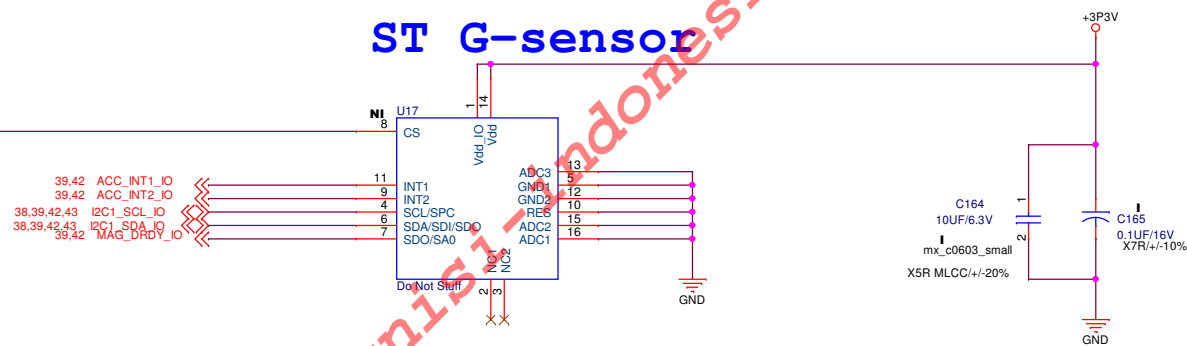
- a. If possible, please avoid using any through-hole.
- b. Please make the trace length short, and the trace width wide enough.
- c. The spacing to the closest neighbor should be wide enough.

PRESSURE SENSOR

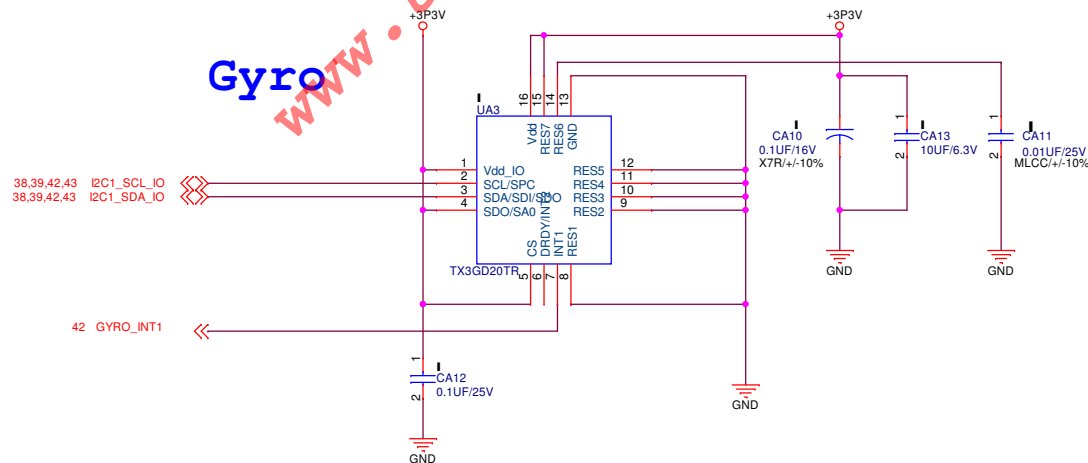


ST G-sensor

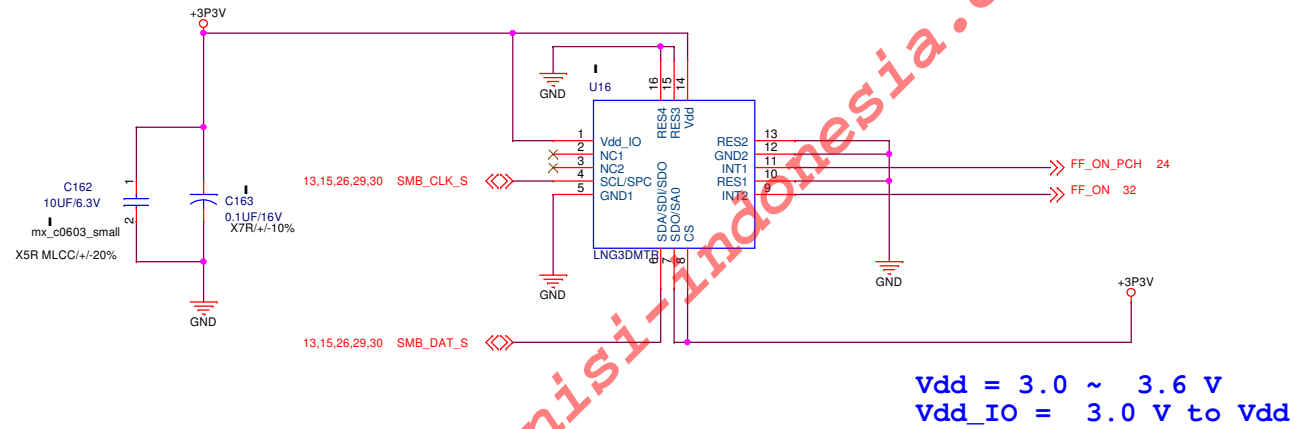
I2C/SPI mode selection
1: I2C mode
0: SPI enabled

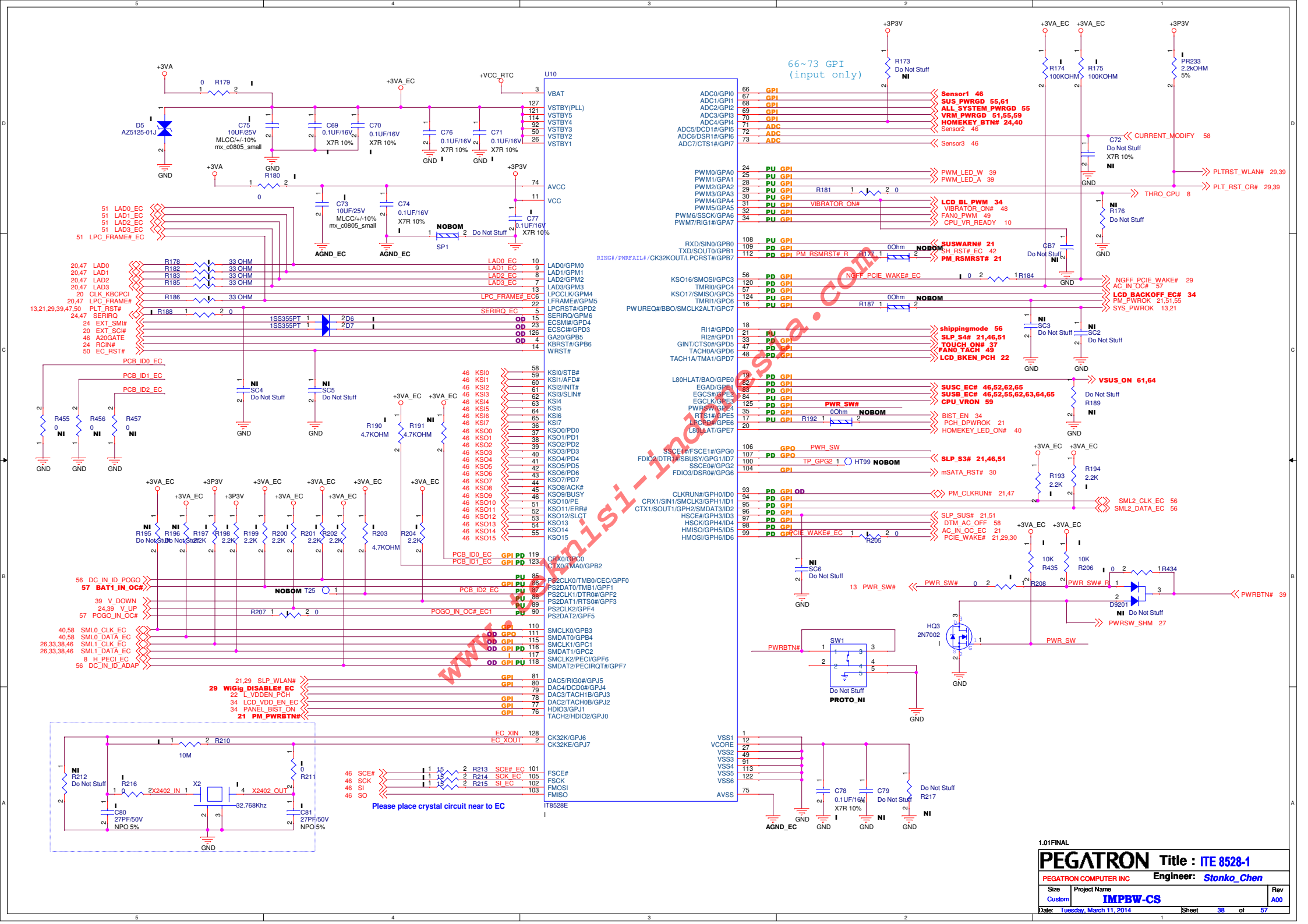


Gyro

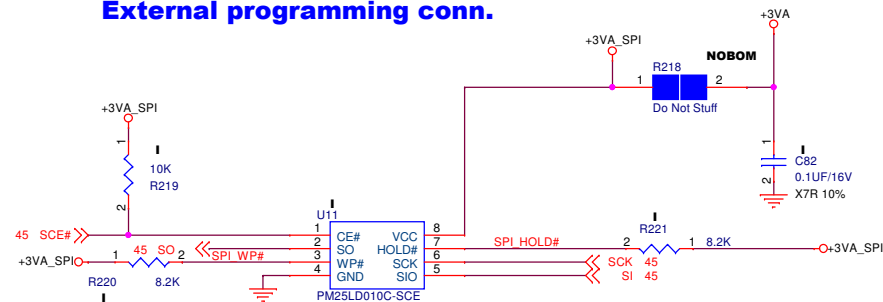


FFS





SPI ROM+ External programming conn.

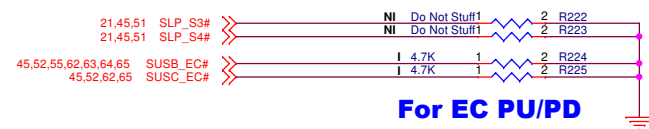


Touch PAD(deleted)

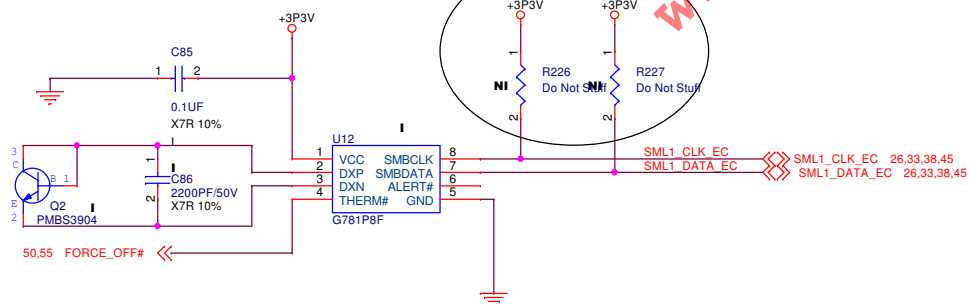
05X0022FC330 32Mb
0500-00P5000 (512Kb SPI)

For Instant Key & Switch

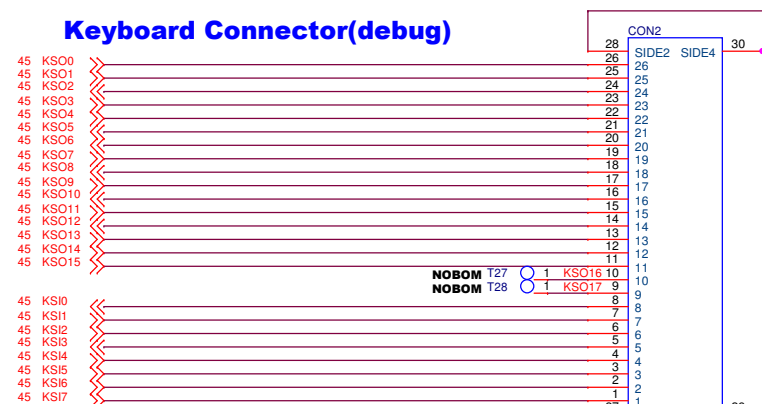
Note: Close to EC



place under DIMM



Keyboard Connector(debug)



Debug Card CON

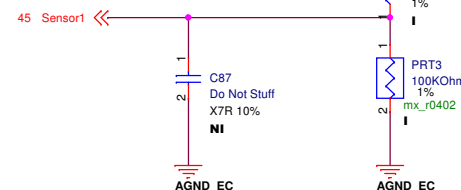
Sensor2:INTAKE (PRT7)



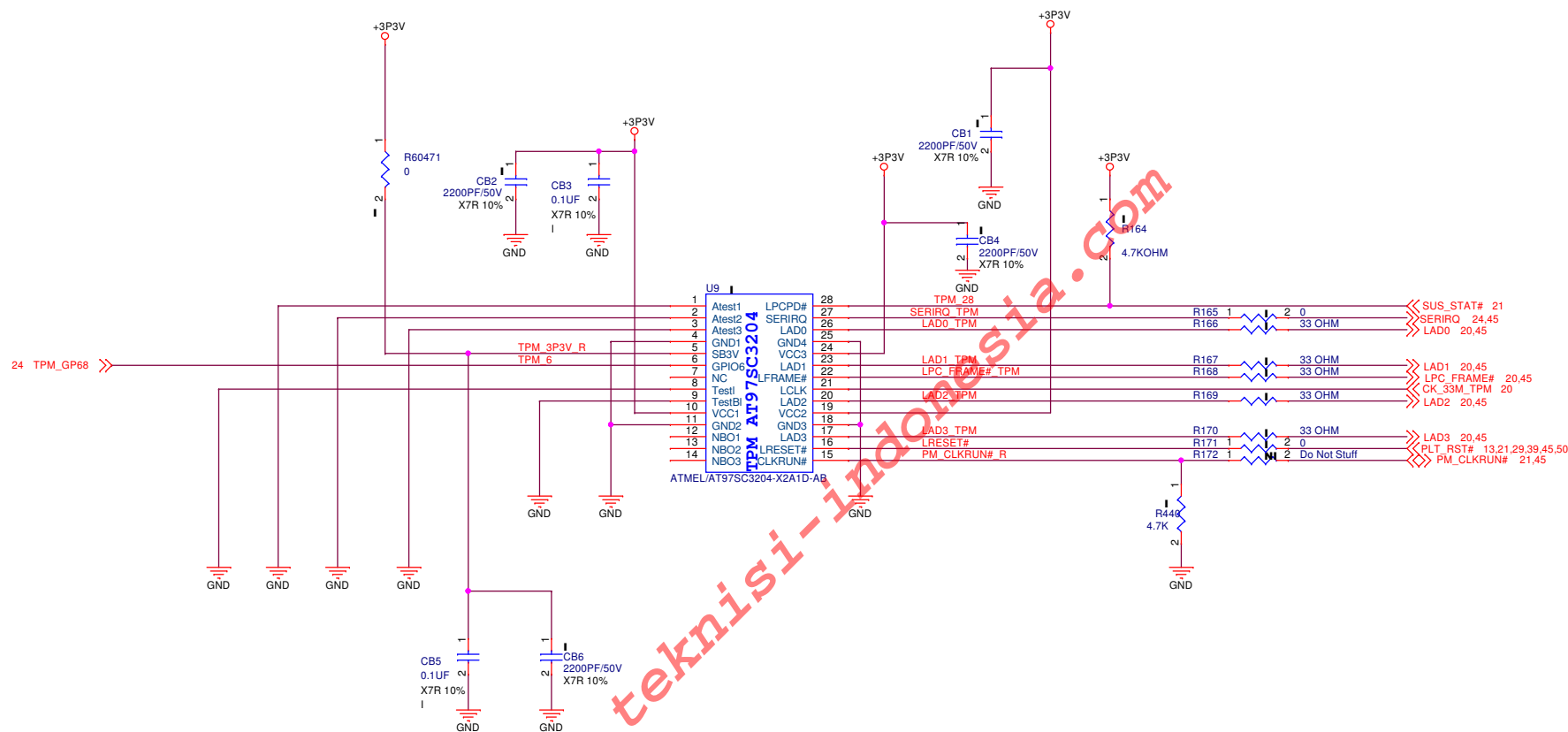
close DIMM (PRT9)



靠近風扇



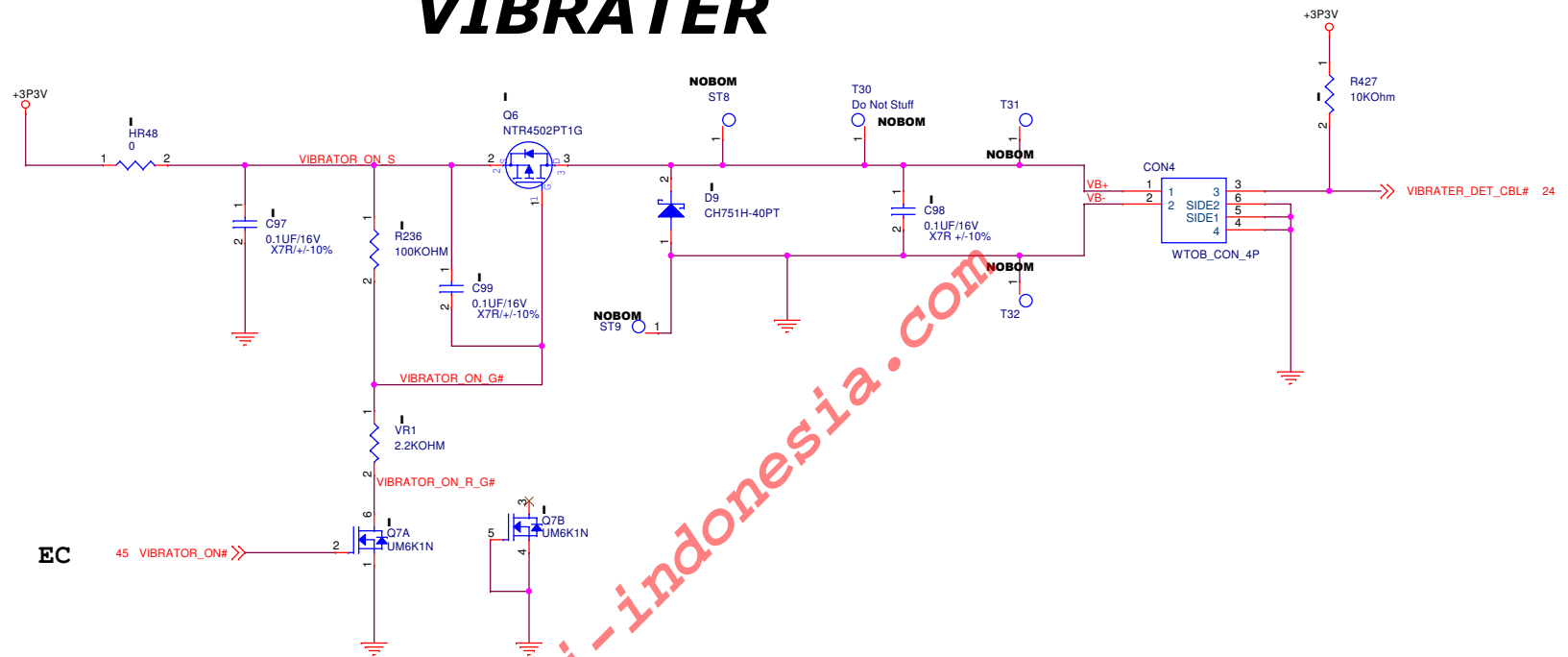
1.01FINAL



1.01FINAL

PEGATRON		Title : TPM	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS		Rev A00
Date: Tuesday, March 11, 2014		Sheet 40 of 57	

VIBRATOR



EC

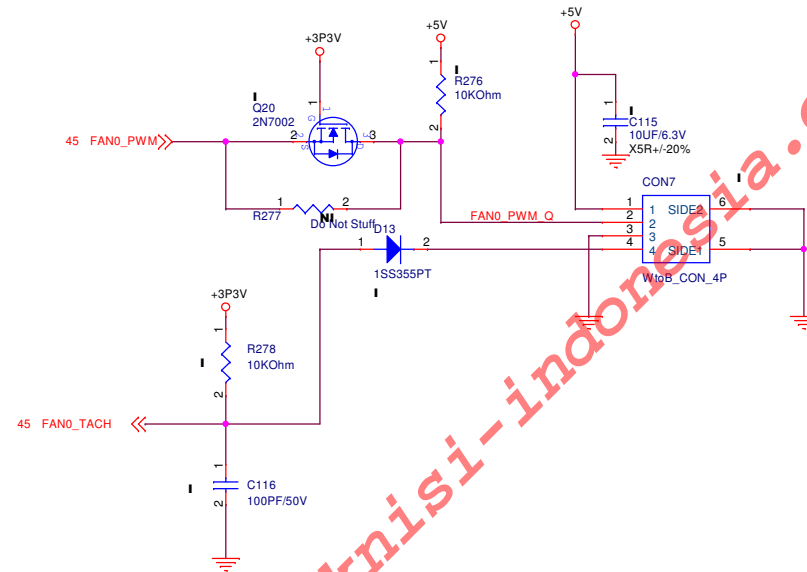
45 VIBRATOR_ON# >>

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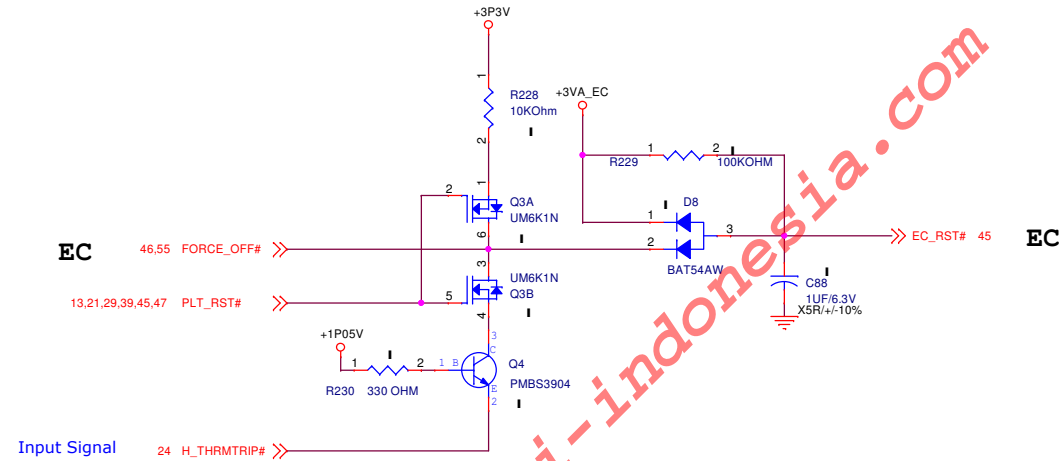
1.01FINAL

PEGATRON		Title : VIBRATOR	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS	Date: Tuesday, March 11, 2014	Rev A00
Sheet 41 of 57			

PWM FAN



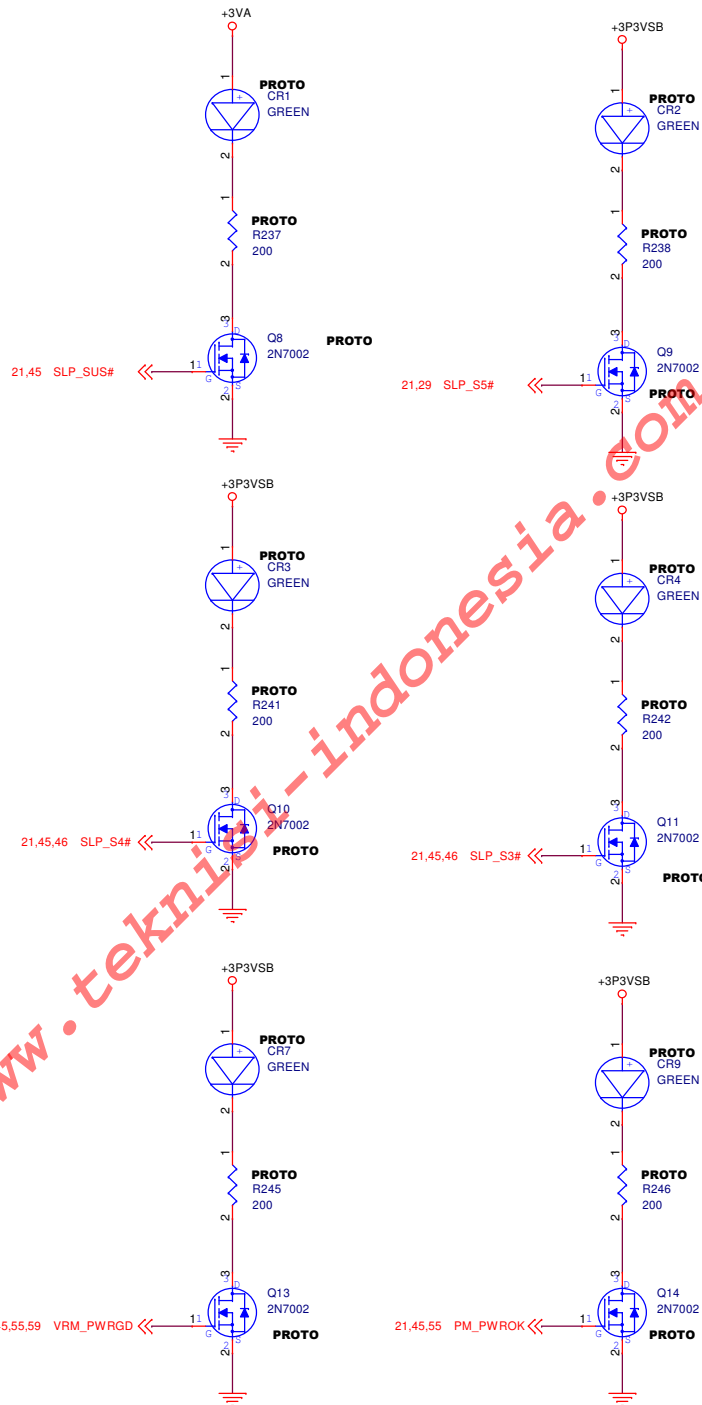
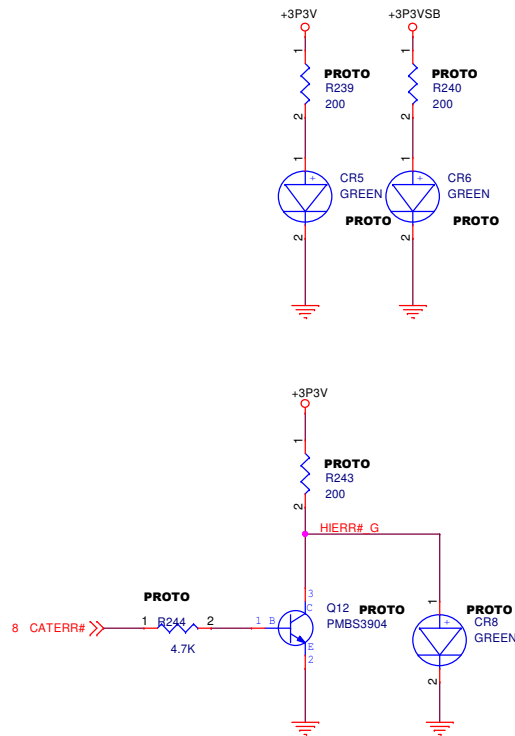
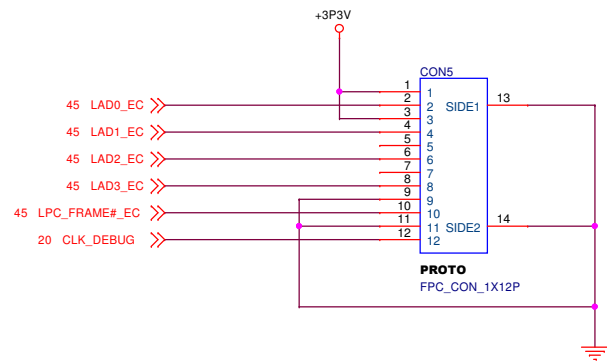
Thermal Policy



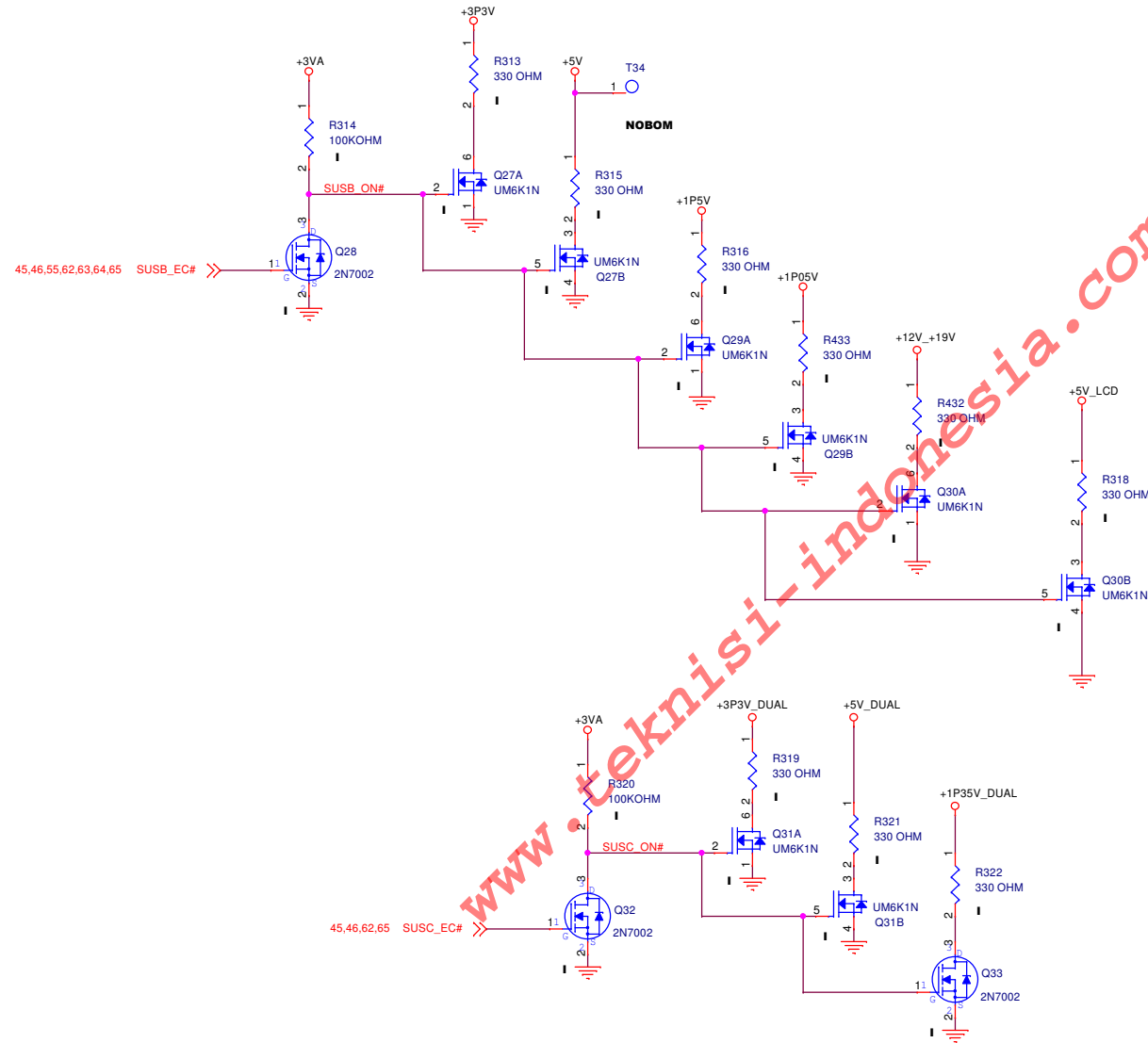
1.01FINAL

PEGATRON		Title : RST_Reset Circuit	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS	Rev A00	
Date: Tuesday, March 11, 2014		Sheet 43 of 57	

DEBUG CARD CONN.

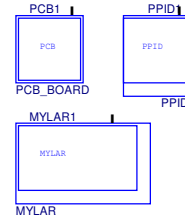


Discharge Circuit

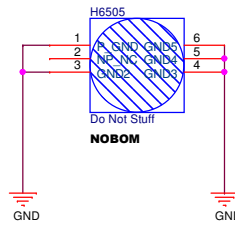


1.01FINAL

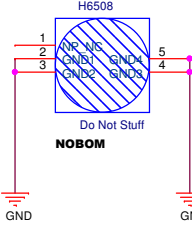
PEGATRON		Title : DSG_Discharge	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS	Rev A00	
Date: Tuesday, March 11, 2014		Sheet 45 of 57	



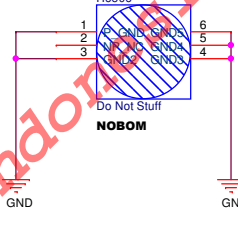
close fan



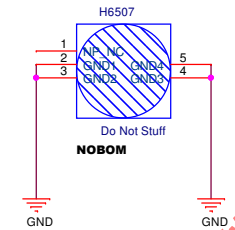
center



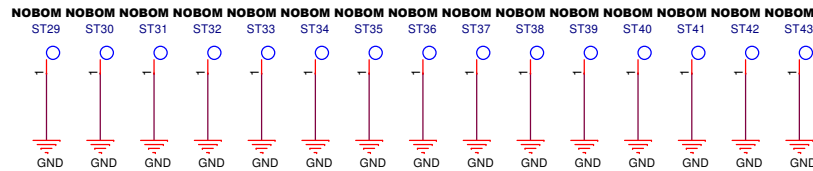
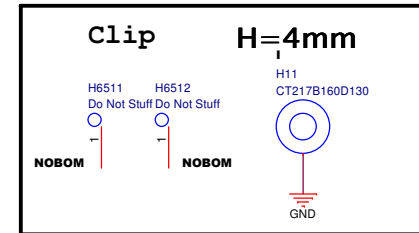
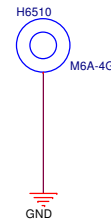
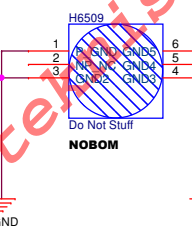
close CON5102



GND close L-IO



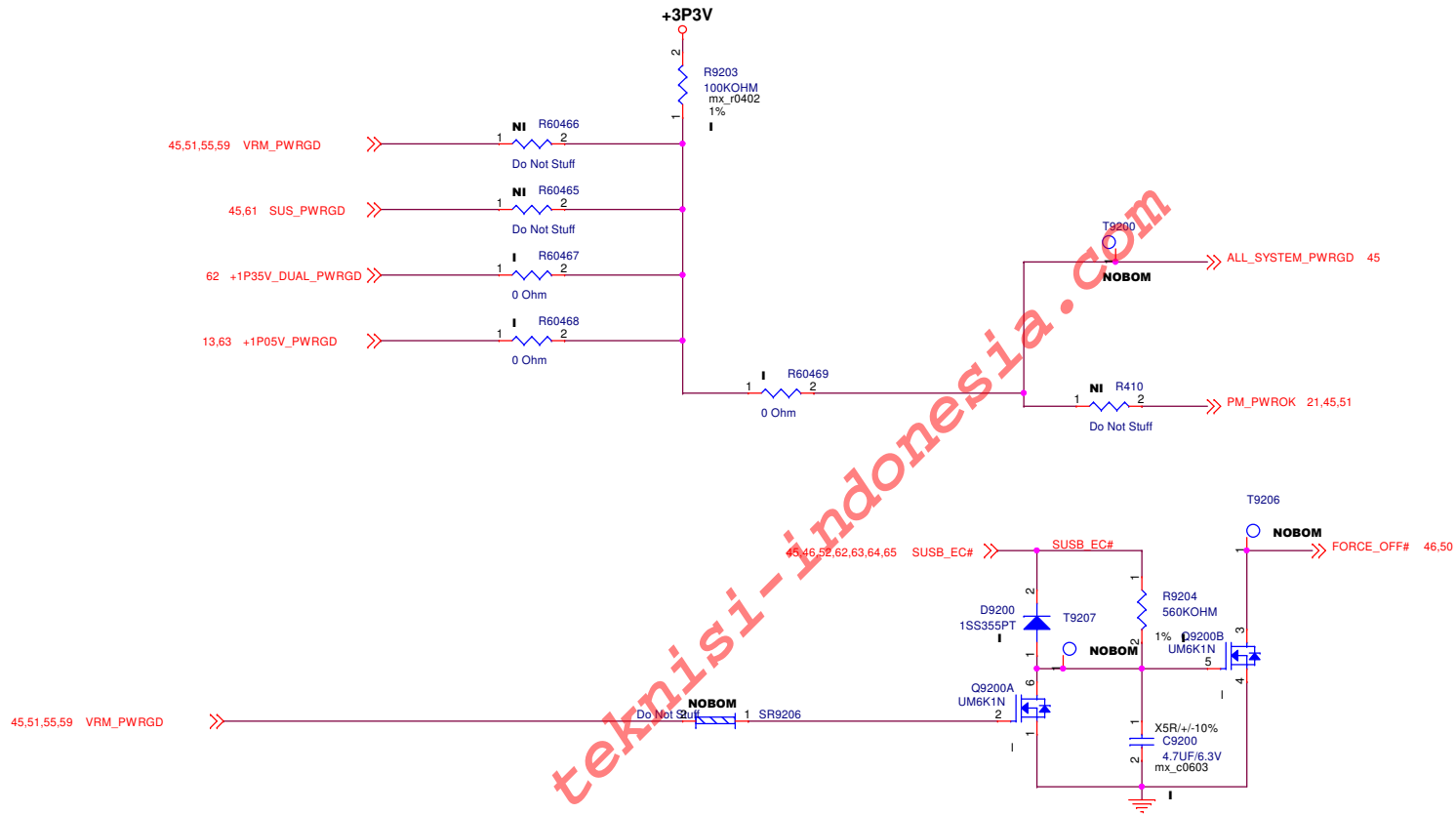
close R-IO



1.01FINAL

PEGATRON		Title :	screw
PEGATRON COMPUTER INC		Engineer:	Stonko_Chen
Size A3	Project Name IMPBW-CS	Rev A00	
Date: Tuesday, March 11, 2014		Sheet	46 of 57

POWER GOOD DETECTOR



1.01FINAL

POGO PIN

+A/D_DOCK_IN 3.5A →

3.5A ↑

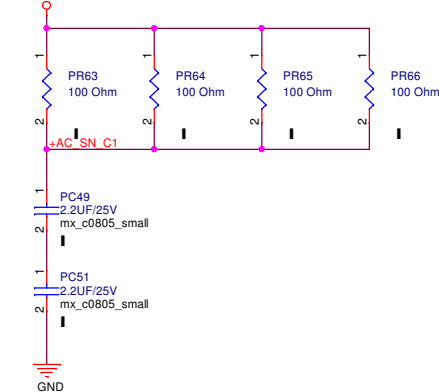
3.5A ←

DC Jack

DC IN

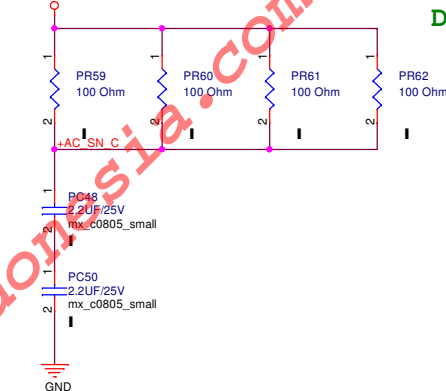
+Adapter_IN

+A/D_DOCK_IN



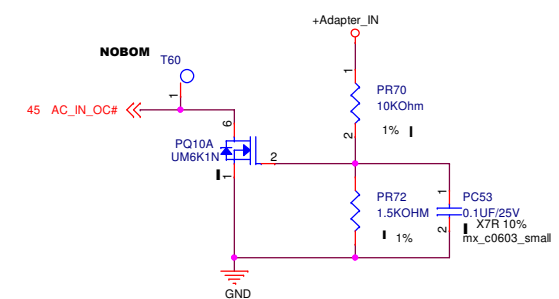
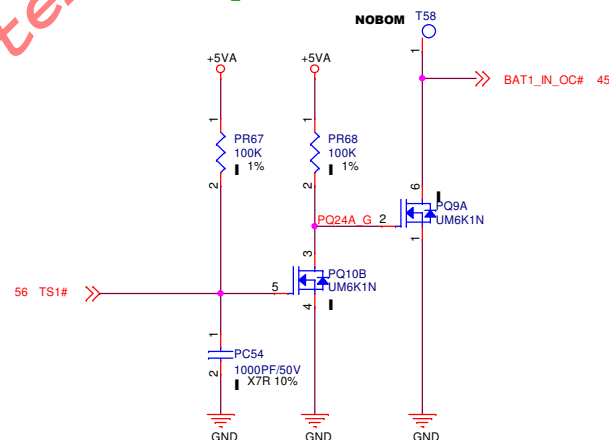
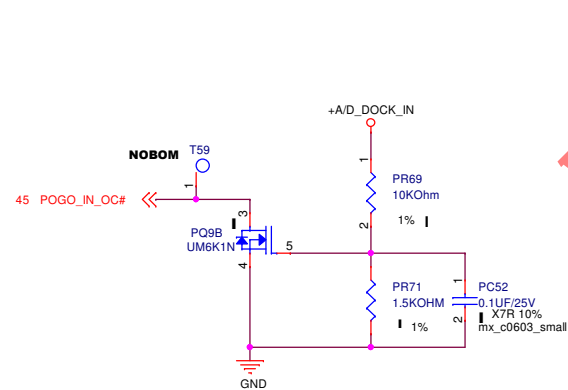
+Adapter_IN

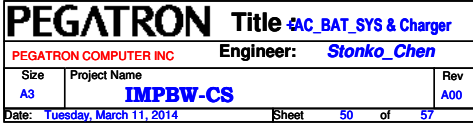
DOCKING IN DETECT

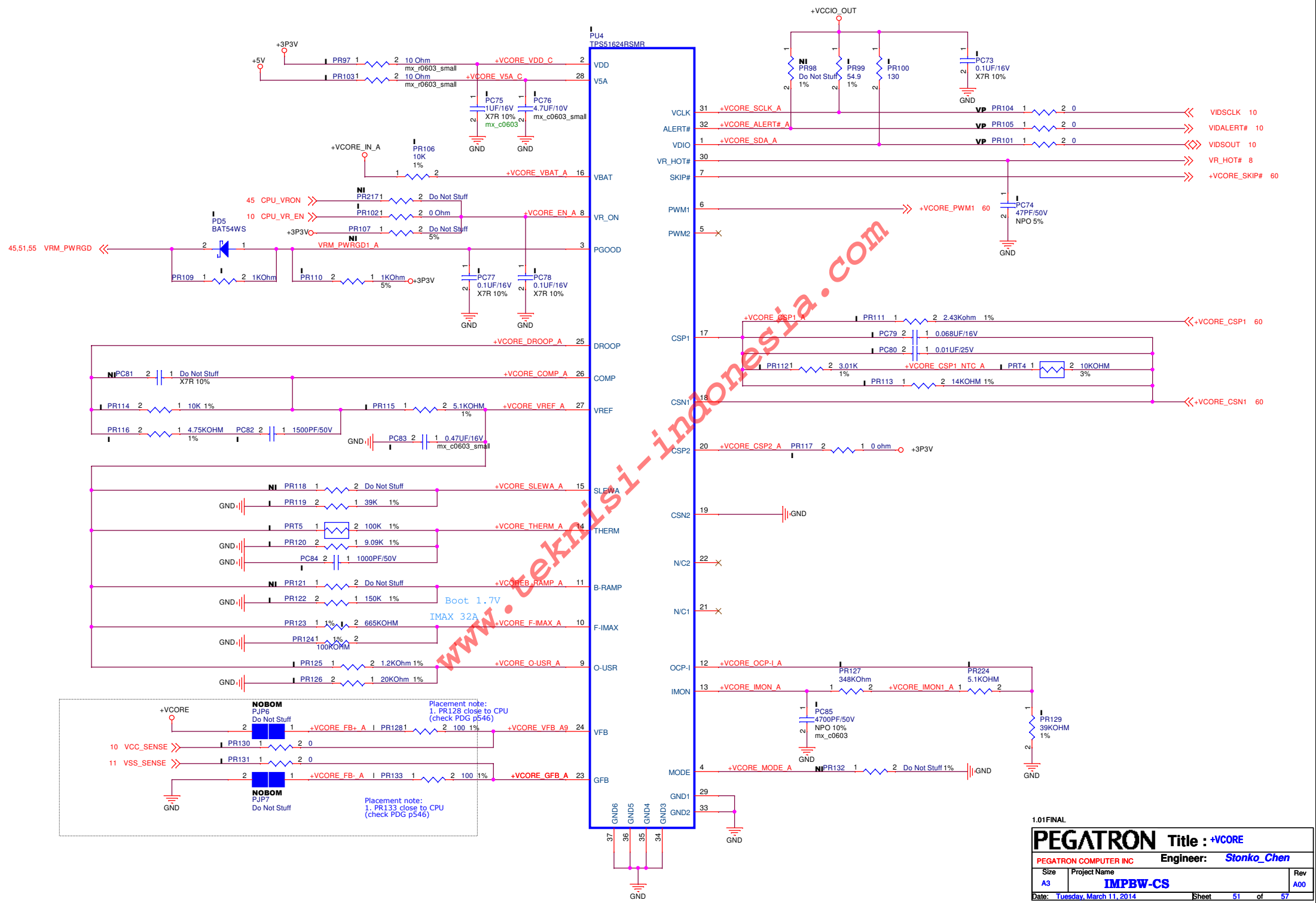


Battery IN DETECT

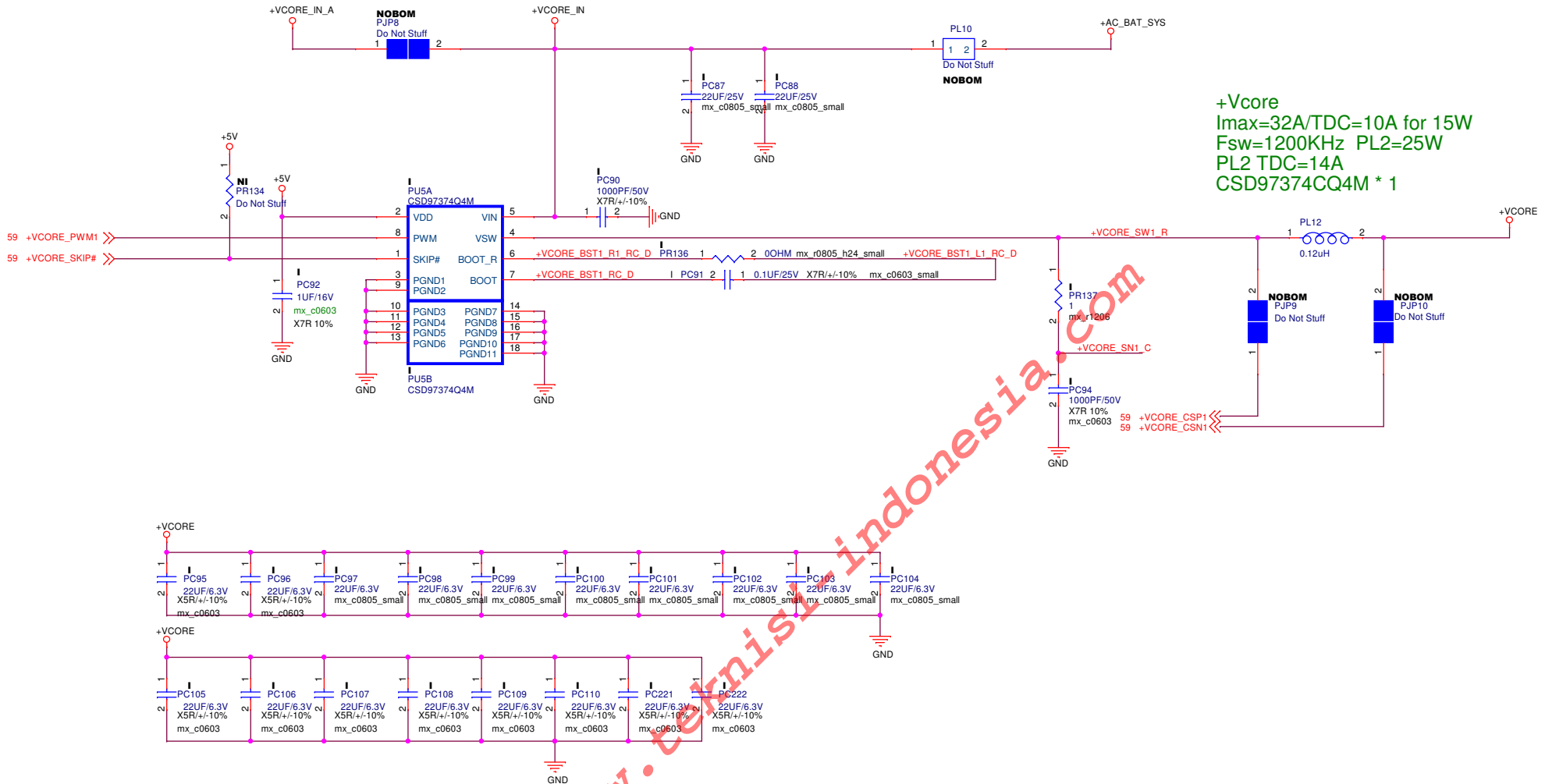
ADAPTER IN DETECT







Iin 2.6A when PL2=25W 60s



+Vcore
I_{max}=32A/TDC=10A for 15W
F_{sw}=1200KHz PL2=25W
PL2 TDC=14A
CSD97374CQ4M * 1

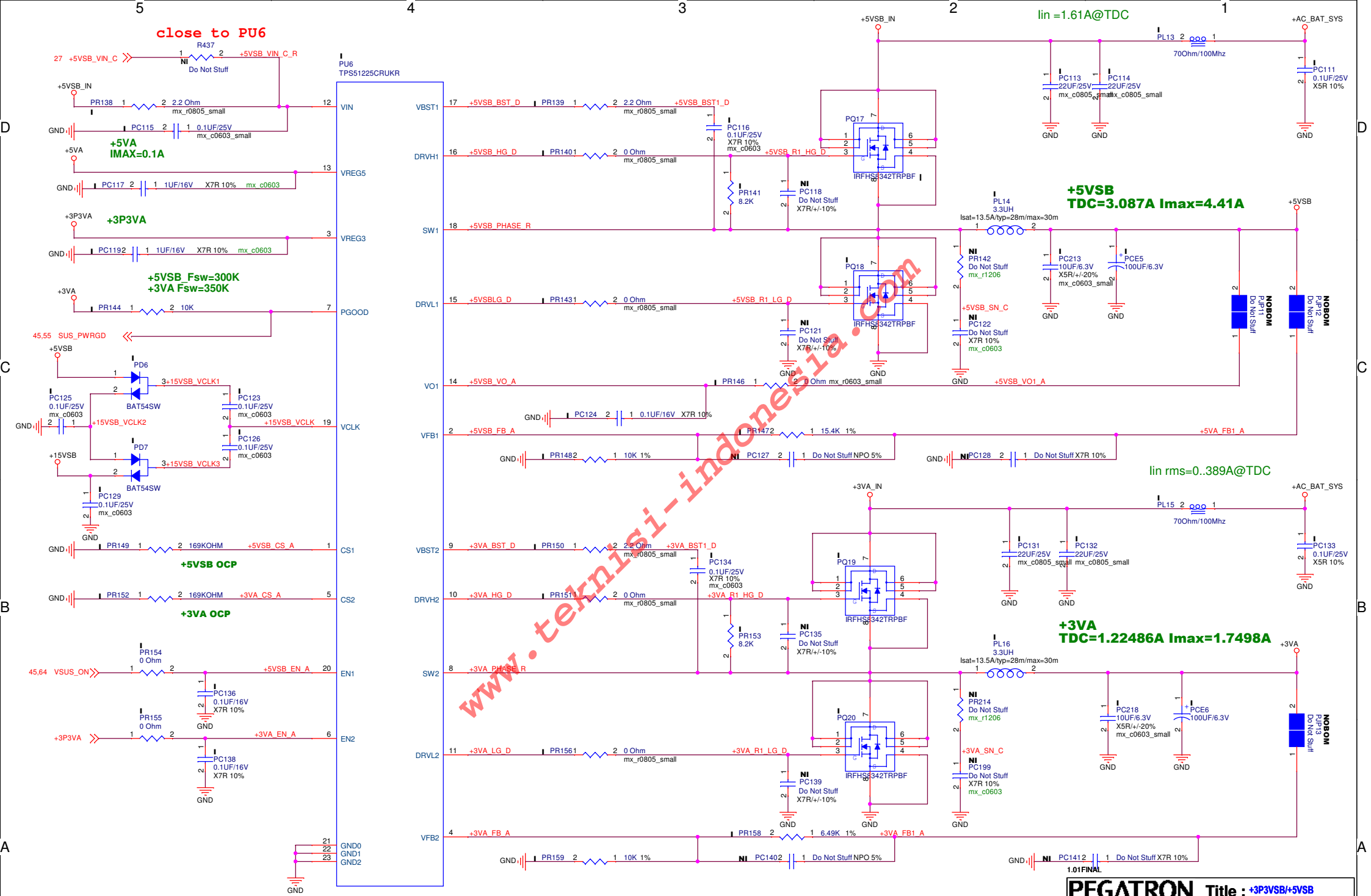
Table 51-15. Broadwell U VccIn Decoupling Recommendations

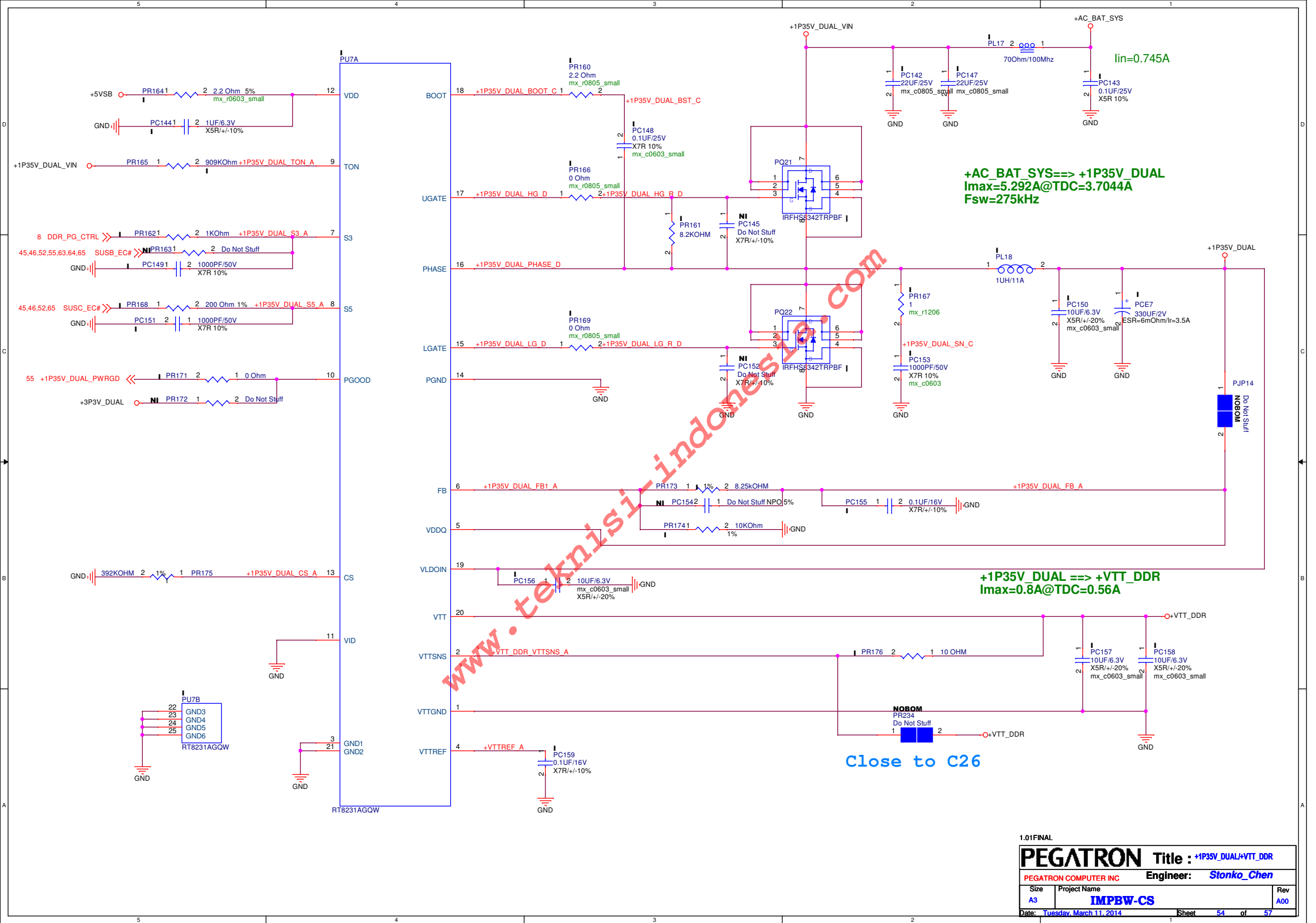
Processor TDP	Inductor size	Size Type	C, μ F	ESR, m Ω	ESL, nH	Supplier or PN
15W	0.47 μ H	0805 X5R	22 μ F 23x - Stuff 7x - no-stuff	3 m Ω	0.6 nH	TDK, Kyocera, Murata, Taiyo-Yudae, Samsung
28W			22 μ F 26x - Stuff 4x - no-stuff			

Note: See the manufacturer data sheet for more details.

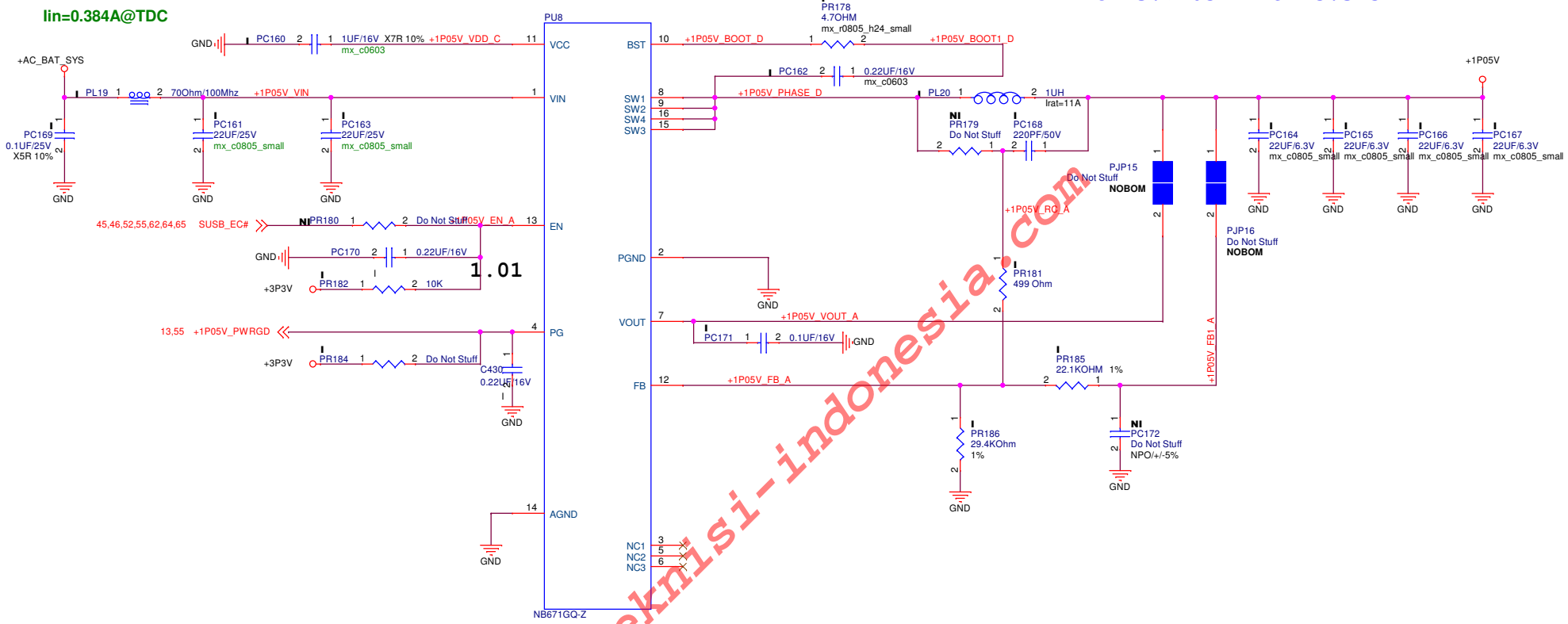
1.01FINAL

PEGATRON Title : +Vcore1	
PEGATRON COMPUTER INC Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS
Date: Tuesday, March 11, 2014	Sheet 52 of 57



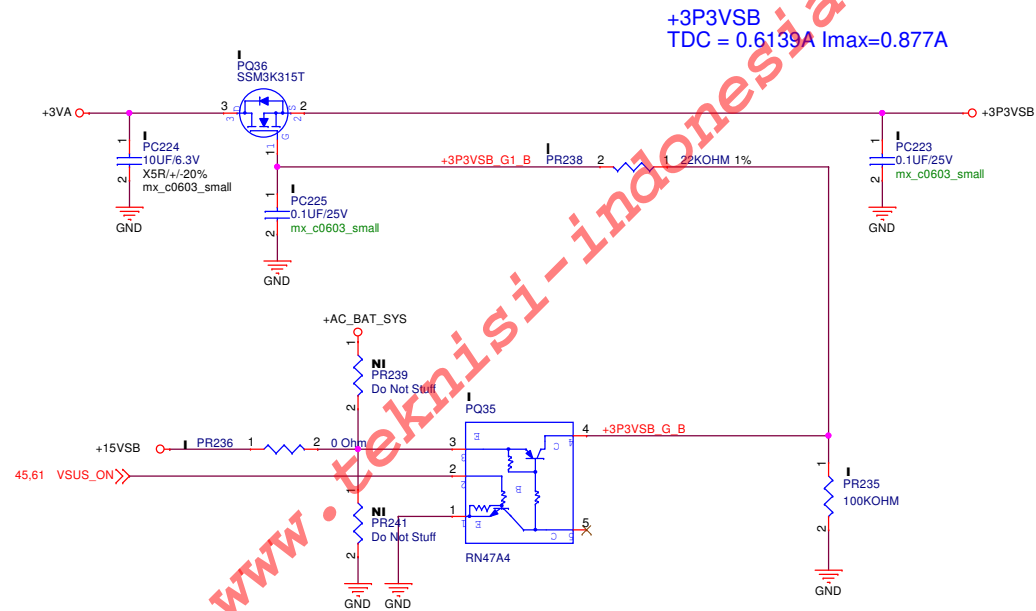
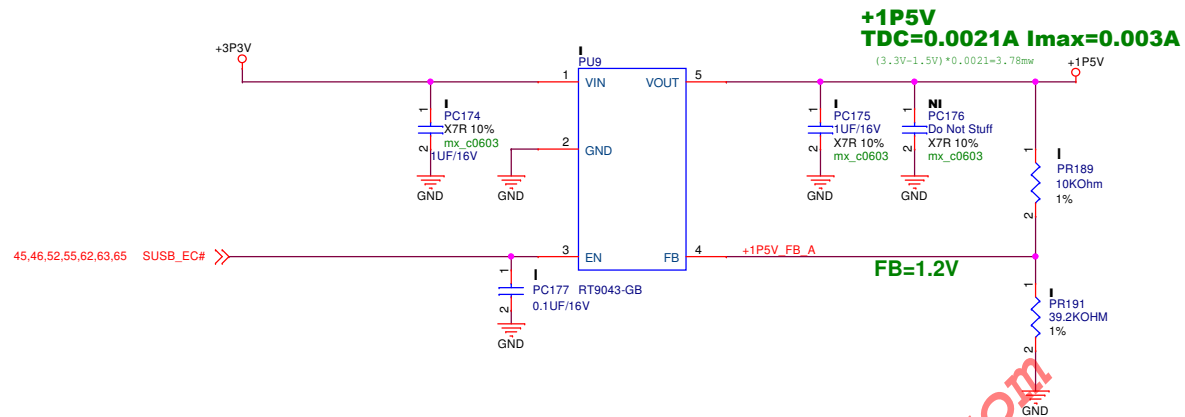


+1P05V
TDC =3.7205A I_{max}=5.315A



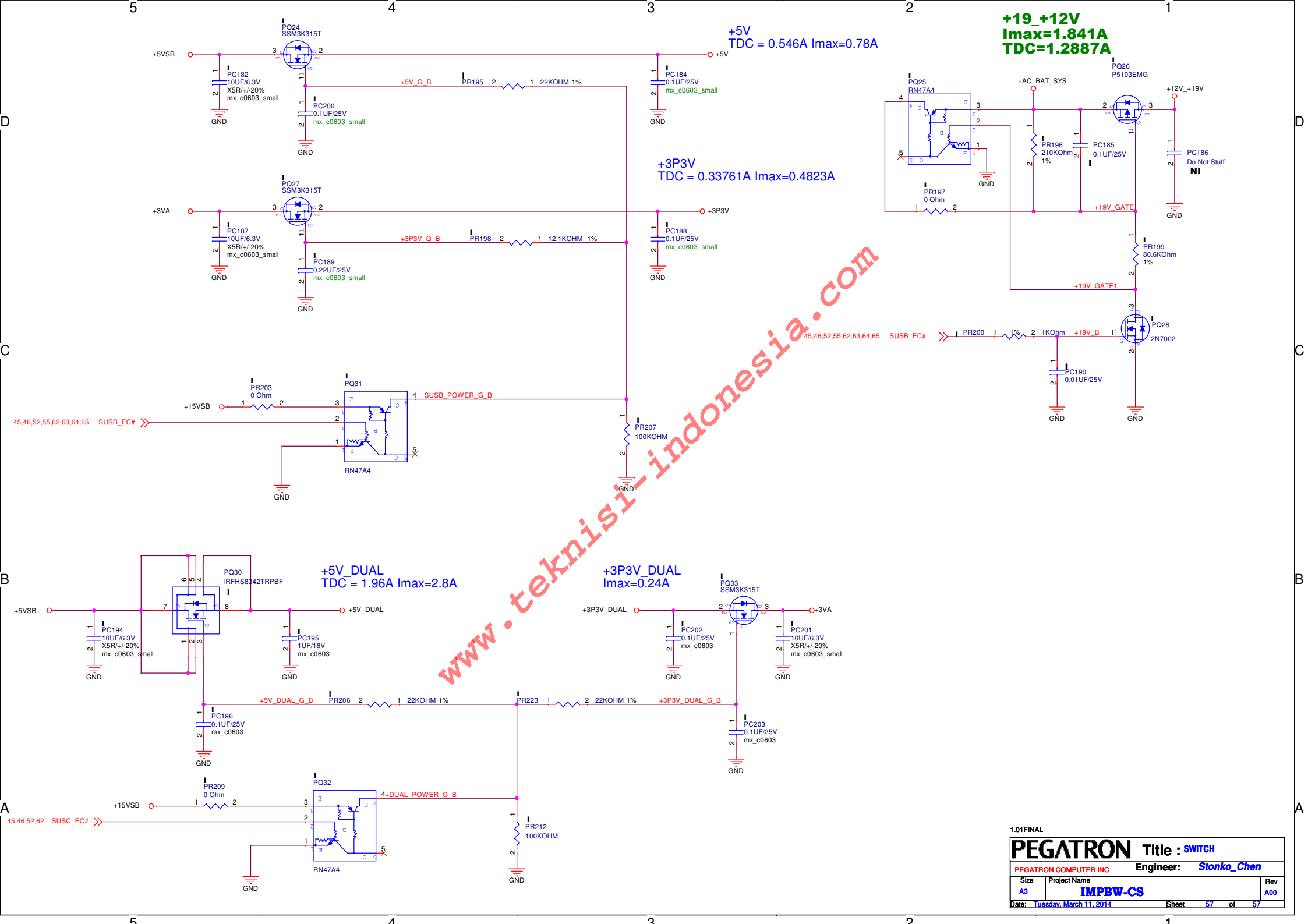
1.01FINAL

PEGATRON		Title : +1P05V	
PEGATRON CORPORATION		Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS		Rev A00
Date: Tuesday, March 11, 2014		Sheet 55 of 57	



1.01FINAL

PEGATRON		Title : +1P5V +3P3VSB	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size	Project Name	Rev	
A3	IMPBW-CS	A00	
Date: Tuesday, March 11, 2014		Sheet 56 of 57	



+5V
TDC = 0.546A I_{max}=0.78A

+19 +12V
I_{max}=1.841A
TDC=1.2887A

+3P3V
TDC = 0.33761A I_{max}=0.4823A

+5V_DUAL
TDC = 1.96A I_{max}=2.8A

+3P3V_DUAL
I_{max}=0.24A

1.01FINAL			
PEGATRON		Title : SWITCH	
PEGATRON COMPUTER INC		Engineer: Stonko_Chen	
Size A3	Project Name IMPBW-CS		Rev A00
Date: Tuesday, March 11, 2014		Sheet 57 of 57	